PXA270-10
Card Engine

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Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
A	Nathan Kro	Release	--	KTL	04/27/05
B	James Wicks	Doc Edit , Removed “Preliminary” Watermark	--	JAW	04/29/05
C	Nathan Kro	Updated 1.7.1, 3.2.1 Updated LCD signals Added pull up note to UARTA_TX and uP_nIRQD	--	KTL	07/01/05
D	James Wicks	Section 5.4.2, changed Pin 52 description from “LCD Data 8” to “LCD Data 9”	PN 1000076 Rev A	KTL	07/12/05
E	Nathan Kro	Updated 5.2: changed active level of uP_USB2_OVR_CRNT from high to low; changed uP_USB2_OVR_CRNT description from “device” to “host”; changed active level of uP_USB2_PWR_EN from low to high; changed active level of uP_USB1_PWR_EN from high to low; Removed “Active high” from BUFF_DIR_DATA description; Updated Figure 2.2, added “Marvell PXA270 Processor”	PN 1000076 Rev A	KTL	08/26/05
F	Michael Aanenson	- Corrected ‘Symbol’ name for DC IO and Peripheral Supply Voltage to 3.3V_IN in the Absolute Maximum Ratings Table. - Updated Recommended Operating Conditions Table. - Added Typical Power Scenarios table (Section 1.7.1.2) - Added ‘Supported Features’, ‘Overview’, and ‘References’ to peripheral hardware Section 2. - In Section 2, made corrections to the Overview for Memory Mapped CF and Video sections. - Corrected SD_CLK net name in Section 2.2 - Added text to section 3.2.1 regarding use of uP_nRESET_OUT vs. MSTR_nRST signal for external device reset. - Added ‘Basic Power Supply and Reset Design’ block diagram to section 3.5 (Power Management). - Added text to section 3.5.1.3 (3.3V_IN) regarding control of this signal and proper use for external peripherals connected to the Card Engine. - Updated 3.3V_IN signal description in section 5.1 (J1C Connector SO-DIMM 144 Pin Descriptions) - Updated uP_nRESET_OUT signal description in section 5.1 (J1C Connector SO-DIMM 144 Pin Descriptions) - Updated 3.3V_uP_BATT signal description in section 5.1 (J1C Connector SO-DIMM 144 Pin Descriptions) - Changed “Card Engine Rev” to “Schematic Rev” in the Revision History Table to associate revision of HW Spec to revision of Schematic	PN 1000076 Rev A	MAA	05/22/06
G	Jed Anderson	Updated Hirose PNs in Section 6.1 to reflect available parts; Added second Important Note to Section 6.1; General grammatical and formatting changes	PN 1000076 Rev A	JCA	11/03/06
H	Jed Anderson	- Section 1.2: Updated Acronyms list. - Section 1.3: Renamed “Scope of Document” and added text. - Removed Section 1.4 “SOM Advantages”. - Removed Section 3.5.3 “Peripherals” because it contained redundant information already in Section 3.5.1; moved table from Section 3.5.3 to Section 3.5.1. - Section 5.1: J1C Pin #23 changed pull-up resistor from 10K to 33K; J1C Pin #47 changed to an output; Pin #19, 107, and 144 descriptions added requires a minimum of 300 uF bulk capacitance. - Section 5.2: J1A Pin #17 and 18 changed description to specify “software” generally instead of LogicLoader specifically ; J1A Pin #67 description added signal pull down information. - Throughout: General grammatical and formatting changes; Updated Intel references with Marvell.	PN 1000076 Rev A	MAA	08/31/07

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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PRODUCT BRIEF:
Logic :: Marvell

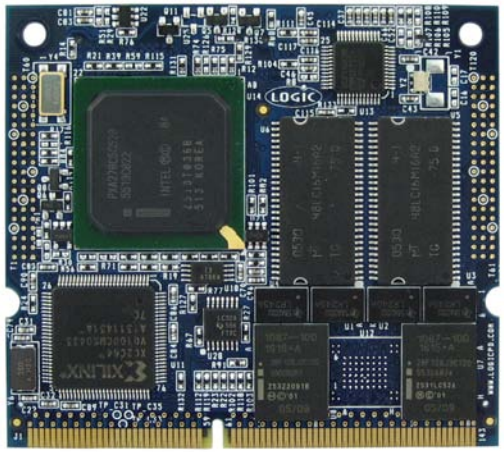
PXA270 CARD ENGINE System on Module

The PXA270 Card Engine is a compact, product-ready hardware and software solution that fast forwards your embedded product design.

The PXA270 Card Engine is a complete System on Module (SOM) that offers essential features for handheld and embedded networking applications. Use of custom baseboards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables easy scalability to next generation microprocessor Card Engines when new functionality or performance is required.

Application development is performed right on the product-ready PXA270 Card Engine and software Board Support Packages (BSPs), which enables you to seamlessly transfer your application code and hardware into production.

The PXA270 Card Engine is ideal for applications in the medical, point-of-sale, industrial, and security markets. From patient monitoring and medical imaging, to card payment terminals and bar code readers, to CCTV cameras and intruder alarms, the PXA270 Card Engine allows for powerful versatility and long-life products.



PXA270 CARD ENGINE

PXA270 CARD ENGINE :: HIGHLIGHTS:

+ Product-ready System on Module with the Marvell PXA270 Applications Processor running at 312, 416, or 520 MHz
+ Compact form factor 60.2 mm x 67.8 mm x 4.4 mm
+ Long product lifecycle
+ 0 ˚C to 70 ˚C (commercial temp) or -40 ˚C to 85 ˚C (industrial temp)
+ RoHS compliant

PXA270 ZOOM™ SDK :: FEATURES:

+ Application baseboard
+ PXA270 Card Engine (CENGPXA270-520-10-504HCR)
+ Necessary accessories to immediately get up and running
+ Kit available from Logic (SDK-PXA270-520-10-6432R)
+ See Zoom™ SDK product brief for more information

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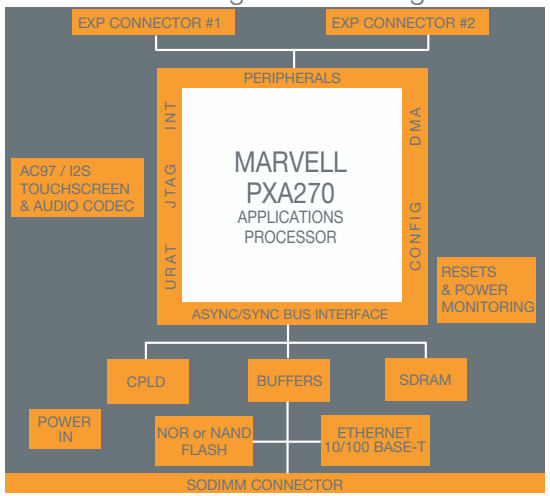
PXA270 Card Engine Block Diagram



PXA270 Card Engine Ordering Information

Logic Model Number	Speed (MHz)	SDRAM (MB)	NAND Flash (MB)	NOR Flash (MB)	Touch	Audio	Ethernet	Temp (°C)
CENGPXA270-312-10-550ECR	312	64	64	0	Y	Y	–	0 – 70
CENGPXA270-416-10-550EIR	416	64	64	0	Y	Y	–	-40 – 85
CENGPXA270-416-10-550HIR	416	64	64	0	Y	Y	Y	-40 – 85
CENGPXA270-520-10-504HCR	520	64	0	32	Y	Y	Y	0 – 70
CENGPXA270-520-10-550HCR	520	64	64	0	Y	Y	Y	0 – 70

PXA270 ZOOM™ SDK Ordering Information

Logic Model Number	SOM Configuration	Recommended Resale
SDK-PXA270-520-10-6432R	CENGPXA270-520-10-504HCR	$499

LOGIC WEBSITE :: DESIGN RESOURCES:

+Logic Technical Support : http://www.logicpd.com/support/
+Technical Discussion Group : http://www.logicpd.com/support/tdg/
+Frequently Asked Questions (FAQ) : http://www.logicpd.com/support/faq/
+For more information contact Logic Sales : product.sales@logicpd.com

LOGIC
embedded product solutions
411 N. Washington Ave. Suite 400 Minneapolis, MN 55401
T : 612.672.9495 F : 612.672.9489 I : www.logicpd.com

MARVELL®

Product Features

Processor
+Marvell PXA270 Applications Processor running at 312, 416, or 520 MHz

SDRAM Memory
+64 MB SDRAM standard

Flash Memory
+Choice of 64 MB NAND or 32 MB NOR

Display
+Programmable color LCD controller
+Built-in driver supports up to 800x600 with 16-bit LCD interface

Touch Screen
+Integrated 4-wire touch screen controller

Network Support
+10/100 Base-T Ethernet controller for application/debug (SMSC LAN 91C111)

Audio
+AC97audio codec

PC Card Expansion
+CompactFlash Type I card (memory-mapped mode only)
+Smart Card, MMC/SD, dual PCMCIA interfaces

USB
+USB 2.0 full-speed host and device interface

Serial Ports
+Three 16C550 compatible UARTs, two I2C

IrDA
+SIR supports up to 115.2 Kbps, multiplexed IrDA/Bluetooth

GPIO
+Programmable I/O depending on peripheral requirements

Software
+LogicLoader™ (bootloader/monitor)
+Windows Embedded CE 5.0 BSP

Mechanical
+60.2 mm wide x 67.8 mm long x 4.4 mm high

RoHS Compliant

PN: 1001781 Rev C

1.2 Acronyms

ADC	Analog to Digital Converter
BSP	Board Support Package
CCCR	Core Clock Configuration Register
CPLD	Complex Programmable Logic Device
DMA	Direct Memory Access
ESD	Electrostatic Discharge
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit Sound
IC	Integrated Circuit
IDC	Insulation Displacement Connector
I/O	Input/Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MMC	Multi Media Card
MMU	Memory Management Unit
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card Internation Association (PC Cards)
PHY	Physical Layer
PLL	Phase Lock Loop
PWM	Pulse Width Modulation
RTC	Real Time Clock
SDIO	Secure Digitial Input Output
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System-on-Chip
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
STN	Super-Twisted Nematic (LCD)
TFT	Thin Film Transistor (LCD)
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface

1.3 Scope of Document

This Hardware Specification is unique to the design and use of the PXA270 SOM as designed by Logic and does not intend to include information outside of that scope. Detailed information about the Marvell PXA270 processor or any other component on the SOM can be found in their respective manuals and specification documents. Specific documents mentioned within this Hardware Specification include:

- PXA270-10 IO Controller Specification (https://www.logicpd.com/auth/)
- LogicLoader™ User's Manual (https://www.logicpd.com/auth/)
- Marvell PXA27x Processor Family Developer's Manual* (http://www.Marvell.com/)
- Marvell PXA270 Processor Electrical, Mechanical and Thermal Specification Data Sheet* (http://www.Marvell.com/)

- Philips UCB1400 AC97 Audio CODEC Data Sheet (http://www.semiconductors.philips.com/)
- SMSC LAN91C111 Data Sheet (http://www.smsc.com/)

*__Note:__ Marvell documents available from their Extranet Portal, which requires registration and approval for access.

1.4 SOM Interface

Logic's common SOM interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common SOM footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic Sales for more information.

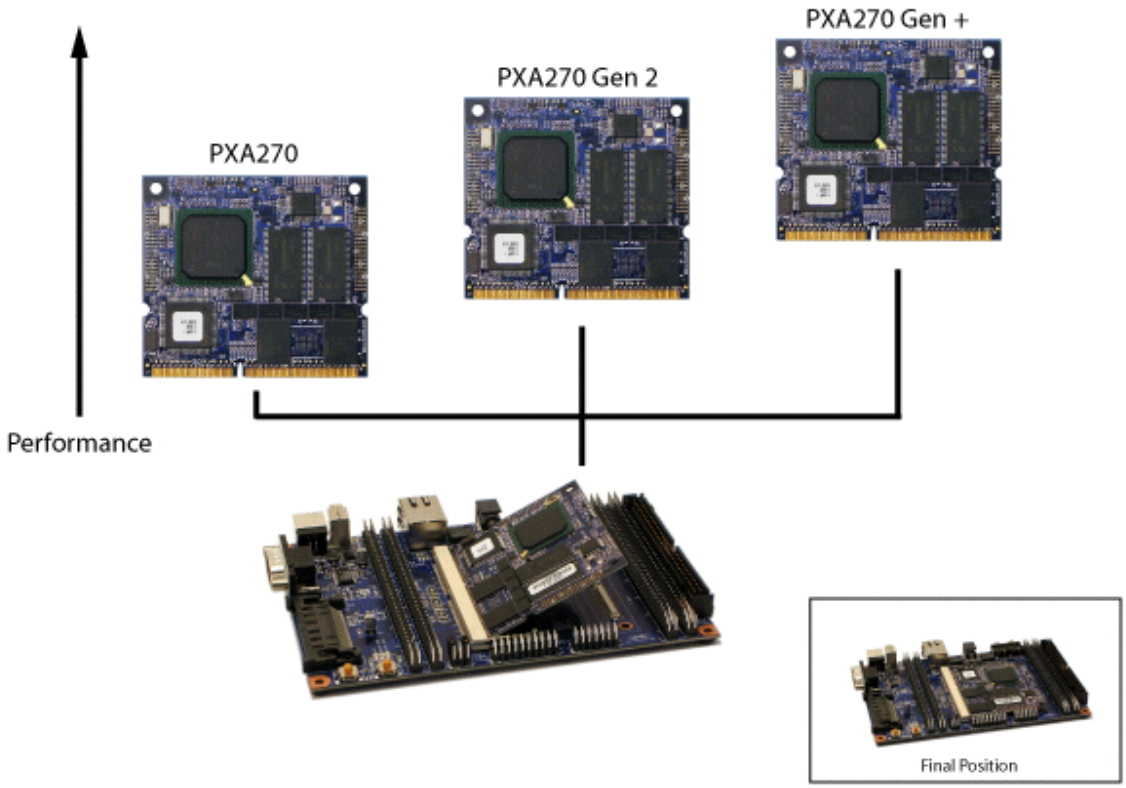


Figure 1.1: SOM Advantages

In fact, encapsulating a significant amount of your design onto the SOM reduces any long-term risk of obsolescence. If a component on the SOM design becomes obsolete, Logic will simply design for an alternative part that is transparent to your product. Furthermore, Logic tests all SOMs prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

1.5 PXA270-10 SOM Block Diagram

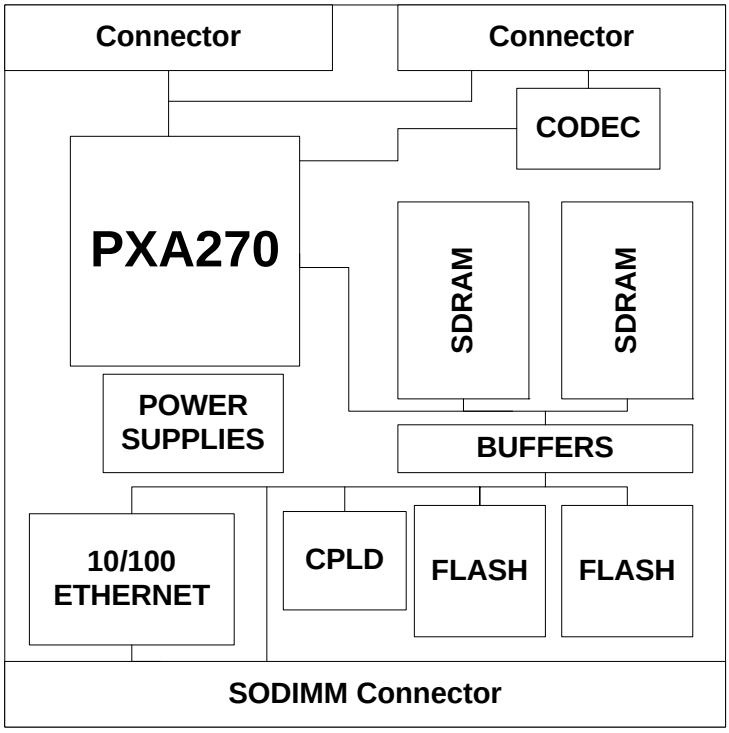


Figure 1.2: PXA270-10 SOM Block Diagram

1.6 Electrical, Mechanical, and Environmental Specifications

1.6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC IO and Peripheral Supply Voltage	3.3V_IN	VSS-0.3 to 3.63	V
DC Battery Supply Voltage	3.3V_uP_BATT	VSS-0.3 to 3.75	V
DC Core Supply Voltage	VCORE	VSS-0.3 to 1.705	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the SOM and its components.

1.6.1.1 Recommended Operating Conditions

The VCORE, SRAM, PLL, and 3.3V power rails are sequenced on the module.

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	7
DC IO and Peripheral Active Current	110	278	—	mA	4,5
DC IO and Peripheral Suspend Current	56	220	—	mA	1
DC IO and Peripheral Standby Current	—	6.6	—	mA	
DC Battery Supply Voltage	3.08	3.3	3.75	V	6,7
DC Battery Supply Active Current	—	—	10	mA	

Parameter	Min	Typical	Max	Unit	Notes
DC Battery Supply Suspend Current	—	—	10	mA	
DC Battery Supply Standby Current	—	21	—	uA	9
DC Core Voltage	1.40	1.45	1.7	V	
DC Core Active Current	260	422	—	mA	4,5,8
DC Core Suspend Current	—	6	—	mA	8
DC Core Standby Current	—	2	—	mA	8
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	2
Storage Temperature	-40	25	85	°C	
Dimensions	—	2.35 x 2.6	—	Inches	
Weight	—	17	—	Grams	3
Connector Insertion/removal	—	50	—	Cycles	
Input Signal High Voltage	0.8 x VCC	—	—	V	
Input Signal Low Voltage	—	—	0.2 x VCC	V	
Output Signal High Voltage	VCC – 0.3	—	VCC	V	
Output Signal Low Voltage	GND	—	GND + 0.3	V	

Notes:

1. Minimum was performed with the 91C111 chip power disabled.
2. Contact Logic for more information on an industrial temperature PXA270-10 SOM.
3. May vary depending on SOM configuration.
4. Minimum is average using WinCE 5.0 BSP with no activity and no display, Ethernet powered.
5. Typical is idle in LogicLoader bootloader with no activity and no display, Ethernet powered.
6. The on-board reset circuit has a reset threshold of 3.08V.
7. 3.3V_IN supply must remain within 200 mV of 3.3V_uP_BATT.
8. Values taken from 520 MHz SOM.
9. Calculated based on Marvell PXA270 and reset chip documentation.

1.6.1.2 Typical Power Scenarios

State	Power	Unit	State Description
Active	1.51	W	LogicLoader, LCDC off, while(1) loop
Ethernet Download	1.63	W	LogicLoader, LCDC off, downloading into RAM
Idle	0.74	W	Windows CE ‘Idle’, LCDC off
Suspend	0.70	W	LogicLoader
Suspend	0.19	W	LogicLoader, Ethernet chip not populated
Standby	0.02	W	LogicLoader, Vcore & 3.3V voltage rails off

2 Electrical Specification

2.1 Microcontroller

2.1.1 PXA270 Microcontroller

The PXA270-10 SOM uses Marvell's highly integrated system on a chip PXA270 microcontroller. This SoC possesses a 32-bit XScale® RISC microprocessor and provides many integrated on-chip peripherals including:

- Integrated Intel XScale® Core
  - 32-bit XScale® RISC Core
  - 32kB Instruction Cache
  - 32kB Data cache
  - 256kBytes on-chip SRAM
  - Memory Management Unit (MMU)
- Integrated LCD Controller
  - Supports up to 800 x 600 and up to 24 bpp format
  - Supports STN, TFT, and Smart Displays
- Three UARTs
- Fast IrDA
- I2C – two channels
- Synchronous Serial Port (SSP) interface – three ports
- I2S or AC97 codec interface
- PC Card Interface – one or two slots
- One USB Client and one USB host interface
- MultiMediaCard / Secure Digital interface
- Keypad interface
- Quick Capture Camera interface
- Pulse Width Modulation (PWM)
- 120 General Purpose I/O (GPIO) signals *(Multiplexed with peripherals signals)
- Multiple independent Direct Memory Access (DMA) channels
- Timers – four Operating System channels, eight independent channels
- Real Time Clock (RTC)
- Low power modes
- Adaptive frequency scaling

See Marvell's *PXA27x Processor Developer's Manual* for additional information.
http://www.Marvell.com/

IMPORTANT NOTE: Please see http://www.Marvell.com/ for errata on the PXA270.

2.1.2 PXA270 Microcontroller Block Diagram

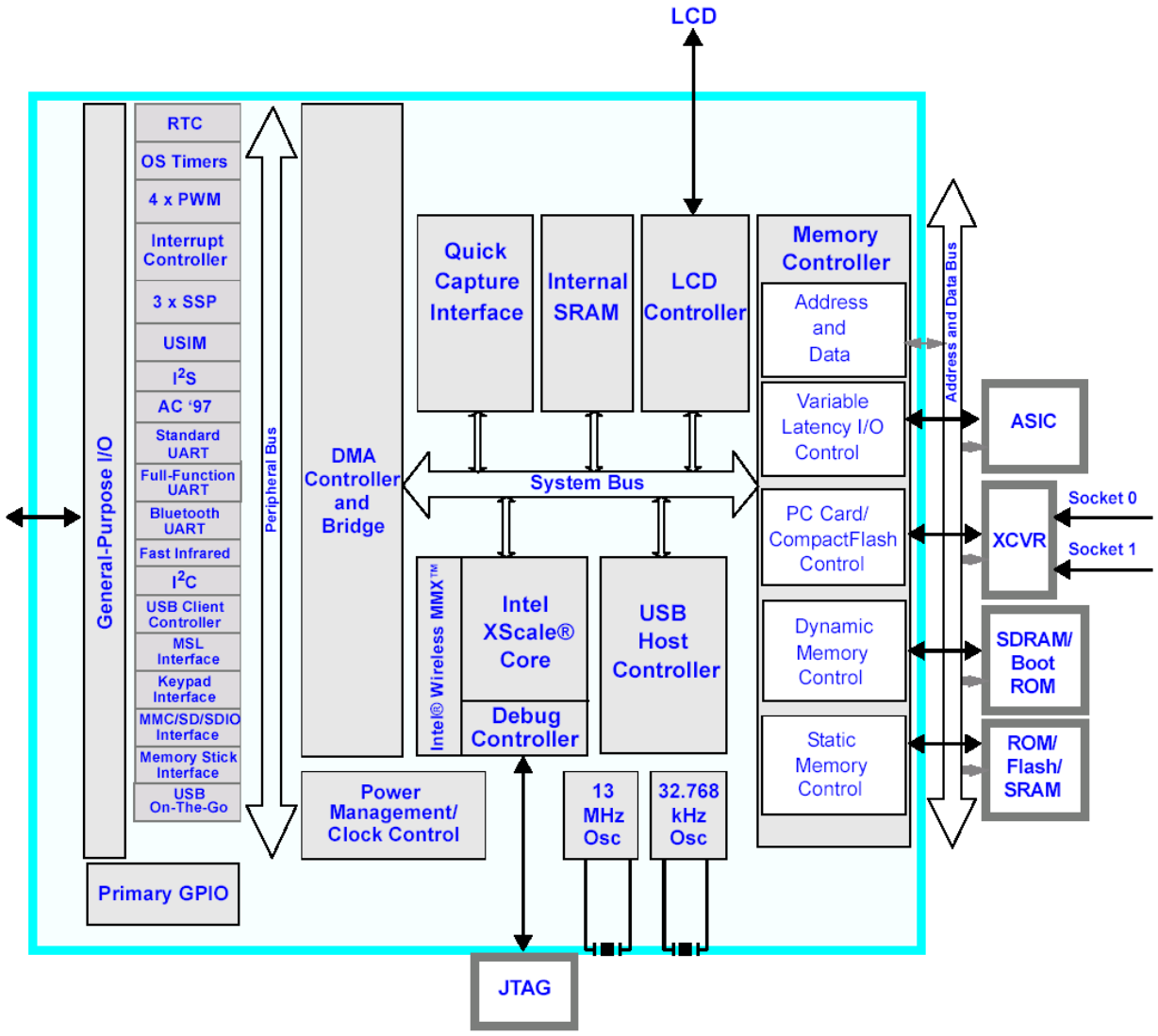


Figure 2.1: PXA270 Microcontroller Block Diagram

2.2 Clocks

The PXA270 requires two crystals in order to enable proper internal timing. A 13.000 MHz crystal is used to generate many of the processor's internal clocks via a series of phased lock loops (PLLs) and signal dividers. To generate the CORE CPU clock the 13.000 MHz signal is run through a PLL controlled by the Core Clock Configuration Register (CCCR). Multiple divisors are used to divide down the internal bus frequency to set the LCD, Memory Controller, Quick Capture interface, and DMA controller. A second PLL is used to create a 312 MHz clock which all peripheral clocks are derived from.

IMPORTANT NOTE: Please see Marvell's *PXA27x Developer's Manual* for additional information about processor clocking.

The second required crystal runs at 32.768 kHz and is the only permanently running clock in the PXA270 as long as power is supplied. The processor uses the 32.768 kHz clock to sequence

power on and off to the device while transitioning between power states and whenever the 13 MHz crystal PLL is disabled.

The PXA270 microcontroller core clock speed is initialized to 520, 416, or 312 MHz on the SOM, depending on model configuration. The SDRAM bus speed is set at 104 MHz in LogicLoader™. Other clock speeds can be supported and modified in software for specific user applications, like specific serial baud rates.

The PXA270-10 SOM provides an external Bus clock, uP_BUS_CLK, on the 144-pin SODIMM connector. The uP_BUS_CLK, which is connected to the processor's SDCLK0, is set to a default of 52 MHz. SDCLK0 is also used to clock the onboard NAND flash and CPLD interface. SDCLK1 serves as the SDRAM clock on the PXA270-10 SOM.

PXA270 Microcontroller Signal Name	PXA270-10 SOM Net Name	Default Software Value in LogicLoader™
CORE	N/A	520 MHz
Internal bus	N/A	208 MHz
SDCLK1	uP_SD_CLK	104 MHz
SDCLK0	uP_BUS_CLK	52 MHz

2.3 Memory

2.3.1 Synchronous DRAM

The PXA270-10 SOM uses a 32-bit memory bus to interface to SDRAM. The memory can be configured as 16, 32, 64, or 128 MBytes in order to meet the user's memory requirements and cost constraints. Logic's default memory configuration on the SOM included in the Zoom Development Kit is specified as 64 MBytes.

2.3.2 Direct Memory Access

The Marvell PXA270 microcontroller has an internal DMA controller. These channels can be used to interface streams from internal peripherals to the system memory (including USB, SD/MMC, AC97/I2S, etc.). The DMA controller can also be used to interface streams from Memory-to-Memory or Memory-to-External Peripheral using two dedicated external channels. External handshake signals are available to support transfers to/from external peripherals. For more information on using the DMA interface refer to the *PXA27x Developer's Manual*.

2.3.3 NOR Flash

The PXA270-10 SOM uses a 32-bit memory bus (split into two, 16-bit channels, one to each flash memory) to interface to NOR flash memory chips. The onboard SOM memory can be configured as 8, 16, or 32 MBytes to meet the user's flash requirements and cost constraints. Logic's default memory configuration on the SOM included in the Zoom Development Kit is specified as 32 MBytes. Because flash is one of the most expensive components on the PXA270-10 SOM, it is important to contact Logic when determining the necessary flash size for final product configuration. NAND flash is a lower cost alternative that should be considered for final product configuration.

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, CompactFlash, or NAND flash. See the PXA270-10 Development Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 NAND Flash

The PXA270-10 SOM can be configured to boot from and use NAND flash. The product supports 64, 128 Mbytes, and other configurations of NAND flash depending on availability. Please contact Logic for more information.

2.3.5 Memory-Mapped CompactFlash

Supported Features

- Single slot
- CompactFlash memory cards

Non-Supported Features:

- Hot-swappable
- I/O cards (e.g., 802.11, modem cards)

Overview

The PXA270-10 SOM supports a CompactFlash memory-mapped slot that compliments the processor's standard dual PC card support. This interface only supports CompactFlash memory cards and does not support removal or insertion (hot-swappable) while the device is powered. The PXA270-10 SOM uses the on-board CPLD to provide the necessary signals for a CompactFlash memory card interface. The Zoom™ Starter Kit reference design includes this interface. See the *PXA270-10 IO Controller Specification* for further details.

The CompactFlash interface is meant to offer designs extra, internal non-volatile memory storage. When implementing this interface in custom designs, it is recommended to use a single-source CompactFlash vendor to provide cards in order to eliminate the possibility for non-compatible cards.

IMPORTANT NOTE: The CPLD Memory-Mapped CompactFlash interface supports memory-mapped mode only. Use the PXA270 processor's PC card slots for more PC card mode options.

Reference

- The *Zoom SDK App Board Schematic* contains the reference design for this interface. Always check Logic's website for the most up-to-date design files: http://www.logicpd.com/auth/.
- The *PXA270-10 IO Controller Specification*, available on Logic's website.

2.4 PC Card—PCMCIA/CompactFlash

Supported Features

- Single or dual slot(s)
- CompactFlash
- PCMCIA
- I/O cards
- Hot-swappable

Overview

Both PCMCIA and CompactFlash devices are supported by the PXA270 SOM. To handle these devices, the PXA270's static memory controller has allocated two configurable memory banks for PCMCIA and CompactFlash interfaces. The SOM can directly support one PCMCIA/CompactFlash slot and has the capability to interface to a second slot with minimal

external circuitry. Logic provides a reference design for connecting a single slot CompactFlash interface to the SOM. Please contact Logic Support for information about connecting dual slots.

In order to properly take advantage of these features, software parameters need to be set; see Chapter 6.4.4 “PC Card and CompactFlash Interface” in Marvell’s *PXA27x Developer’s Manual* for more information.

Reference

- Contact Logic’s Support team through the available online channels: http://www.logicpd.com/support/. A reference design for connecting a single slot CompactFlash card is available on the Logic website.
- Marvell’s *PXA27x Developer’s Manual*

2.5 Secure Digital (SD) and MultiMediaCard (MMC)

Supported Features

- MultiMediaCard (SDIO)
- Secure Digital (SD) – 1-bit or 4-bit
- Secure Digital IO (SDIO) – 1-bit or 4-bit
- SPI

Overview

The PXA270-10 SOM provides one SD/MMC interface that can be used as an MMC card or SD card. This controller supports the full MMC/SD bus protocol identified in the MMC System Specification 3.2, SD Memory Card Specification Version 1.01, and SDIO Memory Card Specification Version 1.0. The controller can also implement a SPI interface to either card. For more detailed operation and programming operations see the MultiMediaCard Association and SD Card System Specifications, available at www.mmca.org and www.sdcard.org, respectively.

Reference

- Marvell’s *PXA27x Developer’s Manual*

2.6 10/100 Ethernet Controller

Supported Features

- 10/100 Mbps network support
- Full/Half duplex
- Auto-negotiation
- LED output (link, activity)

Overview

The PXA270-10 SOM uses the SMSC 91C111 10/100 single chip Ethernet Controller to provide an easy-to-use networking interface. To facilitate use, six signals from the 91C111 are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LEDs. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides an example circuit schematic in the PXA270-10 SDK Development Kit for reference. Please note the TX+/- and RX+/- pairs must be routed as differential pairs on the printed circuit board (PCB).

IMPORTANT NOTE: The ENEEP signal on the SMSC 91C111 is connected to a zero ohm resistor that is not populated. This is because the ENEEP signal has a weak internal pull-up in the SMSC 91C111 and if the signal is tied low it will disable the serial EEPROM interface.

Reference

- The *Zoom SDK App Board Schematic* contains the reference design for this interface. Always check the website for the most up-to-date design file. It is important to use the provided reference design‘s impedance-matching components and proper routing practices.
- SMSC LAN91C111 Datasheet, available at http://www.smsc.com/

2.7 Audio CODEC

Supported Features

- Input – line-in right/left, MIC-in
- Output – line-out right/left
- Audio sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz

Overview

The PXA270 processor has an internal AC97 controller that is compliant with the Audio CODEC ’97 Component Specification, v2.0. This AC97 Controller implements a 5-pin serial interface to the AC97 Audio CODEC, in this case the Philips UCB1400. From the Philips CODEC on the PXA270-10 SOM the outputs are CODEC_OUTL and CODEC_OUTR. These signals are available from the 80-pin expansion connectors.

IMPORTANT NOTE: See Marvell’s specifications for the AC97 standard.

The Philips CODEC on the PXA270-10 SOM performs full duplex 20-bit CODEC functions and supports variable sample rates from 8-48k samples/second. The Philips chip also has an onboard 24.576 MHz crystal which is used for the AC97 master clock frequency.

IMPORTANT NOTE: The Marvell PXA270 also offers an I2S interface for non-AC97 CODEC devices. This interface provides a digital interface that is multiplexed with the signals from the AC97 controller. If you are looking for a different CODEC option, Logic has previously interfaced different high performance audio CODECs into other SOMs. Contact Logic Support for assistance in selecting an appropriate audio CODEC for your application.

IMPORTANT NOTE: This is the same IC (UCB1400) that the SOM uses for touch screen control and ADC. The UCB1400 is connected to the PXA270 via the AC97 interface. Software created for audio, touch screen, and ADC channels should take into consideration that all three interfaces are using the same chip and will need to share the AC97 interface appropriately.

Reference

- The *Zoom SDK App Board Schematic* contains connection information for non-amplified stereo-in and -out for audio. Always check the website for the most up-to-date design files.
- Marvell’s *PXA27x Developer’s Manual*.
- Philips’ *UCB1400 Datasheet*, available at http://www.semiconductors.philips.com/.

2.8 Video Interface

Supported Features

- TFT – 16-bit or 18-bit
- STN – single/dual scan; mono/color; 4-, 8-, 16-bit
- 800 x 600 max resolution
- Bits per pixels formats: 2, 4, 8, 16, 18, 19, 24, 25
- More feature information can be found in Marvell’s *PXA27x Developer’s Manual*

Overview

Marvell's PXA270 microcontroller has a built-in LCD controller supporting STN (single and dual scan) and TFT panels up to 800 x 600 resolution. See the *PXA27x Developer's Manual* for further information on the integrated LCD controller. The LCD data bits from the PXA270's LCD controller are labeled for use with a 16-bit TFT connection by color-bits through the J1A expansion connector. A table showing this mapping is available in Section 5.2. Although the signals are labeled in this way, all data bits are provided on the J1A expansion connector, supporting 4-, 8-, and 18-bit connections in addition to 16-bit interfaces. Logic has experience interfacing numerous panels of different types and sizes in hardware and software. Please contact Logic for development support. Logic provides several Application Notes to help enable this development; all are available on the website for download.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload. Heavy accessing of slow external memory areas (SRAM / PC CARD) can cause screen 'tearing' when larger resolution displays are used. Interfaces on the PXA270-10 SOM that could affect LCD controller "starvation" are NOR flash, SMSC 91C111 Ethernet, memory-mapped CompactFlash, and PC card, in addition to any external ICs on the PXA270 host bus.

Reference

- The Zoom Display Kits by Logic are "plug and play". These provide a quick way to begin development and are easy to use. Several displays at various resolutions are available. Kits come with reference schematics for display connection.
- Marvell's *PXA27x Developer's Manual*
- Logic's AN 161 *Interfacing LCDs to Logic's SDK Board Application Note*
- Logic's AN 298 *Integrating Custom Displays with LogicLoader Application Note*

2.9 Serial Interface

Supported Features

- Three UARTs – 16550A- and 16750-compatible, slow IrDA support
- Three SSP ports
- Fast IrDA port

Overview

The PXA270-10 SOM comes with the following serial channels: UARTA, UARTB, UARTC, SSP, and Fast IrDA. If additional serial channels are required, please contact Logic's Support channels. In most cases, an external UART IC can be used on the local bus to provide several more ports. UARTA, B, and C support wired serial and infrared communications, supporting a digital encoded output and decoded input without analog processing. The signals off of the SOM are at transistor-transistor logic (TTL) levels and require a level shifter for RS232 voltage levels. Please see the *PXA27x Developer's Manual* for further information regarding serial communications.

Reference

- The *Zoom SDK App Board Schematic* contains the reference design for this interface for RS232 level shifting on UARTA. Always check Logic's website for the most up-to-date design file.
- Marvell's *PXA27x Developer's Manual*.

2.9.1 UARTA

UARTA has been configured to be the PXA270-10 Development Kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses First In First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the SOM are TTL level signals, not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the Development Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2K bits/sec, though it supports all common serial baud rates up to 921kbps. This UART also supports SIR IRDA functionality. UARTA is available off the J1C 144-pin SODIMM connector.

2.9.2 UARTB

Serial port UARTB has dual functionality; its primary function is as an asynchronous 16C550-compatible UART. This UART is a high-speed serial interface that uses FIFO, and it is capable of sending and receiving serial data simultaneously. The signals from the SOM are TTL level signals, not RS232 level. The user is responsible for providing an external RS232 transceiver for RS232 applications. UARTB's baud rate can also be set to all common serial baud rates up to 921kbps.

The UARTB is the Marvell Blue Tooth UART and has only TX, RX, CTS, and RTS signaling options. This UART also supports SIR IRDA functionality. UARTB is available off the J1B 80-pin expansion connector.

2.9.3 UARTC

Like UARTA and UARTB, UARTC supports serial communications. UARTC only has TX and RX functional pins. This UART also supports SIR IRDA functionality. Refer to Marvell's *PXA27x Developer's Manual* for more information on using UARTC. UARTC is available off the J1B 80-pin expansion connector.

2.9.4 SSP/SPI

Supported Features

The SSP interface on the PXA270-10 SOM supports multiple data frame formats:

- Texas Instruments SSI
- Motorola SPI
- National Semiconductor Microwire
- Programmable Serial Ports

Overview

The PXA270 has three SSP ports. Logic brings port 1 off of the SOM as a dedicated SPI port. The other two SSP ports can be used, although peripheral/GPIO trade-offs must be made to access these signals.

Logic software by default does not utilize the SSP port. The signals are brought off-board for customer use. The serial format is used to interface between the parallel data inside the SoC and synchronous serial communications on peripheral devices. The signals are available off the 144-pin SODIMM connector. Please see the *PXA27x Developer's Manual* for further information.

2.10 USB Interface

Supported Features

- USB client
  - USB v1.1 compliant
  - Full-speed, 12 Mbps
- USB host
  - USB v1.1 compatible
  - OHCI 1.0a compatible
  - Low-speed / full-speed
  - Root hub supports two downstream ports

Overview

The PXA270-10 SOM is configured with both USB host and device functionality. The USB device interface is compliant to the USB 1.1 specification and both the OpenHCI 1.0a and Marvell UHCI specifications. This USB client supports full-speed (12 Mbits/sec) operation and both suspend and resume signaling. The USB device interface on the PXA270 is able to transmit, receive data, or control information over the bus, and is available for external use off the J1A 80-pin connector.

The USB host interface is compatible with both the USB 1.1 and OpenHCI 1.0a specifications. This controller also supports both low-speed and full-speed USB devices and features a root hub with two downstream ports. The USB connector signals are available off the J1A 80-pin connector. For more information on using both the USB device and host interfaces, please see the *PXA27x Developer's Manual*.

IMPORTANT NOTE: In order for USB to be correctly implemented on the PXA270-10 SOM, additional impedance matching circuitry is required on the USBP and USBM signals before they can be used. USB 1.1 requirements specify that the impedance on each driver must be between 28Ω and 44Ω. For reference, see the impedance matching circuit on the Logic Zoom SDK application baseboard.

Reference

- The *Zoom SDK App Board Schematic* contains the reference design for both the USB device and USB host interface. Always check the website for the most up-to-date design file.
- Marvell's *PXA27x Developer's Manual*

2.11 ADC/Touch Interface

Supported Features

- 4-wire resistive touch-screen support
  - Position, pressure, plate resistance measurement
  - Interrupt generation
- Three 10-bit ADC channels

Overview

The PXA270-10 SOM uses the Philips UCB1400 Audio CODEC with built-in touch screen controller for a 4-wire resistive touch screen interface and 10-bit analog-to-digital converter (ADC). The four touch screen signals and the three A/D signals are available externally off the J1A and J1B 80-pin connectors. Please see the *PXA270 Developer's Manual* for more information.

IMPORTANT NOTE: This is the same IC (UCB1400) that the SOM uses for audio. The UCB1400 is connected to the PXA270 via the AC97 interface. Software created for audio, touch screen, and ADC channels should take into consideration that all three interfaces are using the same chip and will need to share the AC97 interface appropriately.

Reference

- The *Zoom SDK App Board Schematic* contains connection information for non-amplified stereo-in and -out for audio. The Zoom Display Kits show connections to 4-wire touch screens. Always check the website for the most up-to-date design files.
- Marvell's *PXA27x Developer's Manual*
- Philips' UCB1400 Datasheet

2.12 General Purpose I/O

Logic designed the PXA270-10 SOM to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the SOM that interface to the PXA270, and the Xilinx CPLD. Most of these GPIO pins are interrupt capable while other signals are input or output only -- see the "Pin Descriptions" section of this Hardware Specification for more information on these options. If certain peripherals are not desired, such as the LCD Controller, Chip Selects, IRQs, UARTS, AC97, PCMCIA and CompactFlash, Smart Card Interface, or BMI interface, then multiple GPIO pins become available. Please see the table in Section 5.4, "Multiplexed Signal Trade-Offs," for a list of the available GPIO trade-offs.

2.13 CPLD

Please see the *PXA270-10 IO Controller Specification* for CPLD information. Available for download from: http://www.logicpd.com/auth/.

2.14 Serial EEPROM Interface

Logic designed the PXA270-10 SOM to have a low-cost 4 kbit serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the PXA270 microcontroller via the CPLD through an SPI interface. See Figure 2.2 below. For more information please view the *PXA270-10 IO Controller Specification*.

Figure 2.2: Serial EEPROM Block Diagram

2.15 Expansion/Feature Options

The PXA270-10 SOM was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the 144-pin SODIMM connector and two 80-pin expansion connectors. It is possible for a user to expand the SOM's functionality even further by adding PCI or ISA devices. Some features that are implemented on the PXA270, but are not discussed herein, include: keypad, memory stick, RTC, MSL, FIR, PWM, DC-DC, Quick Capture Interface, and I2S. See the *PXA27x Developer's Manual* and the PXA270-10 SOM schematics for more detail. Logic has experience implementing additional options, including other audio CODECs, Ethernet ICs, co-processors, and components on the SOM boards. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The PXA270-10 SOM was designed to meet multiple applications for specific users and budget requirements. As a result, this SOM supports a variety of embedded operating systems and can support the following hardware configurations:

- Flexible memory footprint: 16, 32, 64, or 128MBytes SDRAM
- Flexible NOR flash footprint: 8, 16, or 32MBytes NOR flash
- Flexible NAND flash footprint: 64, 128MBytes, or larger NAND flash
- Optional SMSC 91C111 10/100 Ethernet controller
- Optional Philips UCB1400 audio codec and touch controller

Please contact Logic for custom hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the PXA270-10 SOM use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems. The MSTR_nRST triggers a power-on reset event to the PXA270 and resets the RTC and power controller.

All hardware peripherals should connect their hardware-reset pin uP_nRESET_OUT signal on the SODIMM connector. Internally all SOM peripheral hardware reset pins are connected to the uP_nRESET_OUT net.

If the output of the reset chip, MSTR_nRST, is asserted (active low), the user can expect to lose information stored in SDRAM. The data loss occurs because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal. The RESET_HIGH signal is used to reset the onboard 91C111 controller, and is the active high output of the reset circuit and is not provided as part of the SOM connector interface.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will cause data corruption and possible temporary system lockup). See Section 3.5, “Power Management,” for further details. The following two conditions will cause a system-wide reset: power-on or a low pulse on the MSTR_nRST signal.

Power-on

At power-on, the MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 0.4V and 3.08V. Once the 3.3V_uP_BATT supply surpasses 3.08V the reset chip will trigger a rising edge of MSTR_nRST after a 140-560ms delay (240ms typical).

Low Pulse on MSTR_nRST Signal

A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that for any external assertion source that triggers the MSTR_nRST signal, analog or digital, de-bouncing be used to generate a clean, one-shot reset signal.

3.2.2 Soft Reset

Logic has created a soft reset signal, SW_nRESET, designated as a reset for the PXA270's internal registers without affecting the peripherals on the rest of the board or the data stored in SDRAM. The data is saved because the SDRAM controller automatically places the SDRAM in self-refresh before the uP_SD_CLK clock is disabled. As in the Standby state described in Section 3.5.4.3, the 32.768 kHz clock continues running, allowing the system to properly wake up. The SW_nRESET signal is an input to the PXA270 processor's GPIO1 input pin.

Figure 3.1: Soft Reset

See Marvell's *PXA27x Developer's Manual* for additional information on register conditions after a soft (manual) reset. A soft reset case triggered by the SW_nRESET signal must be setup in software to support the soft reset function.

3.3 Interrupts

The PXA270 incorporates a two-level hierarchy of interrupts. Primary interrupts come from internal peripherals, secondary interrupts are interrupts specific to a peripheral. Interrupts can be set as standard IRQs or FIQs to change the level of the interrupt. Refer to Marvell's *PXA27x Developer's Manual* for further information on using IRQ and FIQ interrupts. Most GPIO pins can be defined as interrupts so the product can support multiple external interrupt sources.

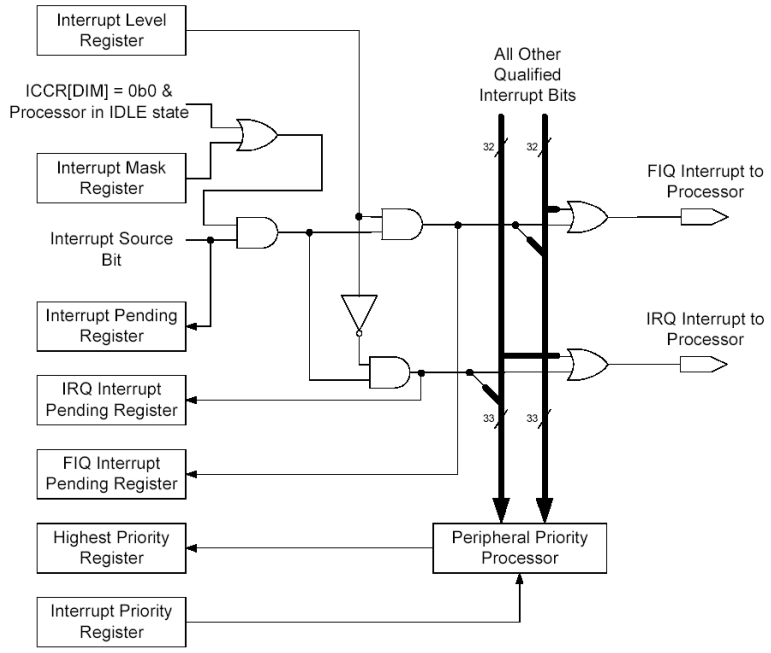


Figure 3.2: PXA270 Interrupt Structure

NOTE: The CPLD interrupts the processor via the GPIO0 signal.

3.4 JTAG Debugger Interface

The JTAG connection on the PXA270 allows recovery of corrupted flash memory and real-time applications debug. When choosing a debugger board, remember that many different third-party JTAG debuggers are available for Marvell microcontrollers. The following signals make up the JTAG interface to the PXA270: uP_TDI, uP_TMS, uP_TCK, and uP_TDO. These signals should interface directly to a 20-pin 0.1" through-hole connector, as demonstrated in the Marvell *PXA27x Developer's Manual* or as shown on reference schematics.

IMPORTANT NOTE: When laying the 20-pin connector out, realize it may not be numbered as a standard 20-pin 0.1" through-hole insulation displacement connector (IDC). See the PXA270-10 SOM Development Kit reference designs for further details. Different IC manufacturers define the 20-pin IDC connector pin-out differently.

3.5 Power Management

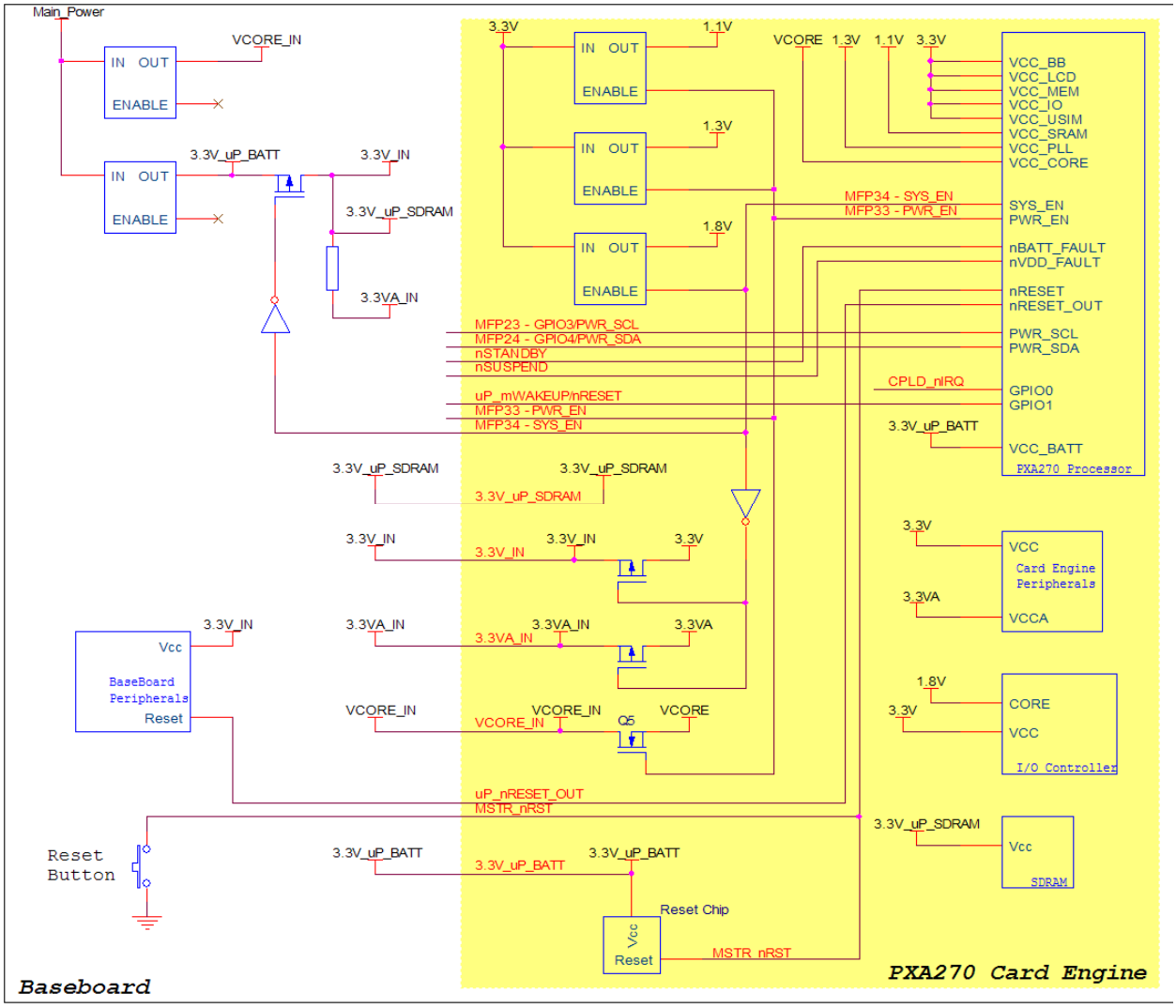


Figure 3.3: Basic Power Supply and Reset Design Block Diagram

3.5.1 System Power Supplies

In order to ensure a flexible design, the PXA270-10 SOM was designed to have the following power areas, 3.3V_uP_BATT, 3.3V_uP_SDRAM, 3.3V_IN, 3.3VA_IN, 3.3V_WRLAN, and VCORE_IN. All power areas are inputs to the SOM with the exception of 3.3V_WRLAN, which is an output from the SOM.

Logic Net Name	Required Input VDC	Notes
3.3V_uP_BATT	3.3V	Connects to the processor VCC_BATT input. This signal provides power to the PXA270 RTC and power management unit. This supply should be active at all times.
3.3V_uP_SDRAM	3.3VDC	Connects to the Processor's 3.3-volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and the SDRAM to self refresh.

Logic Net Name	Required Input VDC	Notes
3.3V_IN	3.3VDC	Connects to the digital peripherals on the SOM. This supply should be used for powering devices connected to the SOM and should be controlled with the SYS_EN signal. Requires at minimum a 300 uF bulk capacitor.
3.3VA_IN	3.3VDC	Connects to the Audio Codec on the SOM to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
3.3V_WRLAN	3.3V (This pin is an output, see Section 3.5.1.4)	Provides power to the SMSC 91C111 processor from the 3.3V area. The power to the 3.3V_WRLAN area is controlled by the signal WRLAN_ENABLE from the CPLD. See the *PXA270 IO Controller Specification* for controlling this signal.
VCORE_IN	1.45-0.8V	Connects to the processor core voltage. See information on each specific processor for the VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, power modes, temperatures, etc.

3.5.1.1 3.3V_uP_BATT

The 3.3V_uP_BATT input pins are connected to a 3.3V power supply with an optional backup battery. This signal powers the PXA270 on-chip Power Management Unit which powers the RTC and controls power up and power down sequencing. This supply should be maintained at all times in order to retain proper RTC time.

3.5.1.2 3.3V_uP_SDRAM

The 3.3V_uP_SDRAM input pins are connected to a 3.3V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SDRAM supply should be maintained above the minimum level at all costs, see Section 2, “Electrical Specification”. Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in this section below.

3.5.1.3 3.3V_IN

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the PXA270-10 SOM. This supply must stay within the acceptable levels specified in Section 2, “Electrical Specification”, unless experiencing power down or critical power conditions. Putting the PXA270 into Deep Sleep mode will turn off the 3.3V power plane.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

The module uses the PXA270 SYS_EN signal to power the 3.3V_IN on and off during the power up and power down sequence. The user should ensure that 3.3V_IN is powered before attempting to transition to the Run state.

The 3.3V_IN supply must be controlled using the SYS_EN signal if any external peripheral is connected to the SOM, including devices connected to the host bus and GPIO signals. The 3.3V_IN supply must be used to power these devices. If this is not done, the devices can come up in incorrect states, as the PXA270 processor’s peripheral connections are not powered yet. Also, the PXA270’s peripheral interface can be back-powered, causing processor life-time issues.

3.5.1.4 3.3VA_IN

The power nets connected to the 3.3VA power plane handles all peripheral supply pins (analog), but not the PXA270 processor on the PXA270-10 SOM. The 3.3VA supply must stay within the acceptable levels specified in Section 2, “Electrical Specification”, unless powering down the board or under critical power conditions. Putting the PXA270 into Deep Sleep mode will turn off the 3.3VA power plane.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

The module uses the PXA270 SYS_EN signal to power the 3.3VA_IN on and off during the power up and power down sequence. The user should ensure that 3.3VA_IN is powered before attempting to transition to the Run state.

3.5.1.5 3.3V_WRLAN

This “power” supply net is an output from the SOM and is controlled through a registered bit in the onboard CPLD. For more details on this specific control bit, see the *PXA270-10 IO Controller Interface Specification*. Logic’s software BSP asserts this signal in order to properly manage power in the LAN91C111 Ethernet chip. However, this management does not put the part in a low enough power state for many applications.

The custom application board should use the 3.3V_WRLAN output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 3.3V directly or the entire Ethernet controller circuit on the SOM will try to power itself through the impedance matching resistors. Please see Logic’s schematics of the Development Kit reference designs for details.

IMPORTANT NOTE: The purpose of the 3.3V_WRLAN power plane on the SOM is to power the 91C111 chip separately and allow for a complete, but independent, shut down. Furthermore, the 3.3V_WRLAN output from the SOM is required to completely isolate the LAN circuit so that it is not back-powered through the impedance matching resistors.

3.5.1.6 VCORE_IN

VCORE_IN is the variable voltage power supply for the VCC_CORE pins on the PXA270. VCORE power-on/off sequencing is controlled on the module by an N channel MOSFET controlled by the PWR_EN signal. The VCC_CORE input can be changed dynamically as the operating frequency changes. Refer to the Marvell EMTS specification for detailed VCC_CORE voltage requirements. Transitioning the PXA270 to Sleep or Deep Sleep modes will disable the VCORE power plane on the module. Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the Standby state. Please see the description of Standby mode later in this section.

3.5.1.7 VCC_SRAM (internal to SOM only)

The module creates a 1.1V power plane for the VCC_SRAM inputs on the PXA270. The 1.1V plane is powered from the 3.3V supply and is enabled by the PWR_EN signal. The VCC_SRAM supply is powered off when the processor is put into Sleep or Deep Sleep mode.

3.5.1.8 VCC_PLL (internal to SOM only)

The module creates a 1.3V power plane for the VCC_PLL input on the PXA270. The 1.3V plane is powered from the 3.3V supply and is enabled by the PWR_EN signal. The VCC_PLL supply is powered off when the processor is put into Sleep or Deep Sleep mode.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The PXA270-10 SOM was designed to keep these aspects in mind and provide maximum flexibility in software and system integration.

On the PXA270 there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes, microcontroller power management states (Run, Idle, Deep Idle, Sleep, Deep Sleep), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel, etc.). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the *LogicLoader™ User's Manual* or appropriate BSP manual.

IMPORTANT NOTE: Most of the PXA270-10 SOM hardware architecture was designed for low-power, battery-operated applications. For optimal control of power, a variable output voltage regulator should drive the VCORE_IN supply. Software can scale the operating frequency with the appropriate VCORE voltage for maximal power savings. The SOM exports two I2C signals from the PXA270 which are intended for power management circuit control. If a user desires voltage scaling power control, please contact Logic Product Development for assistance in implementing the interface.

3.5.3 Microcontroller

The PXA270 processor power management's scheme was designed to be easy to use. There are six power management modes provided in the PXA270 microcontroller: Run, Idle, Deep Idle, Standby, Sleep, and Deep Sleep. Logic Product Development BSPs have simplified the power management scheme to three power states, Run, Suspend, and Standby. Please see below for descriptions from all three states and the *PXA27x Developer's Manual* for more details

3.5.3.1 Run State

Run is the PXA270-10 SOM's normal operating state in which both oscillator inputs and all clocks are hardware enabled. The PXA270 can enter Run mode from any state. From the Standby state, Run can be accessed by a rising-edge on the uP_nWAKEUP/nRESET (GPIO1 on processor) signal or from a predefined internal interrupt source. A Standby-to-Run transition occurs on the assertion of MSTR_nRST or uP_nWAKEUP/nRESET (GPIO1 on processor) signal. A reset occurs during this transition because context was lost when entering the Standby Mode. All power supplies are active at this time.

3.5.3.2 Suspend State

Suspend state is the PXA270 SOM's hardware power-down state, allowing for lower power consumption. The Suspend state is designed to reduce power consumption while the PXA270 is waiting for an event such as a keyboard input. The suspend state is entered using Logic BSPs by asserting the nSUSPEND signal or through software. The PXA270 processor is put into Standby Mode. All power supplies remain active. System context is retained. Internal clocks are stopped except RTC. An internal or external wakeup event can cause the processor to transition back to Run Mode.

IMPORTANT NOTE: Although Suspend consumes less power than Run state, it consumes more power than the Standby state. Thus, on a power failure, the PXA270 system will actually leave the Suspend state and transition to the Standby state (the same thing occurs on a SW_nRESET).

3.5.3.3 Standby State

Standby State is the PXA270 SOM's lowest power state. This state is entered in Logic BSPs by asserting the nSTANDBY signal or through software. The PXA270 processor is put into Deep Sleep Mode. All clocks except the RTC are stopped. System context is lost. Power is removed from all PXA270 and onboard peripherals except the PXA270 VCC_BATT and optionally uP_3.3V_SDRAM if their contents wish to be retained. Internal or external wakeup events can cause transition back to run state. System reboot occurs because context is lost.

3.6 ESD Considerations

The PXA270-10 SOM was designed to interface to a customer's peripheral board. The SOM was designed to be low cost and adaptable to many different applications. The PXA270-10 SOM does not provide any onboard ESD protection circuitry – this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SDRAM Memory Map

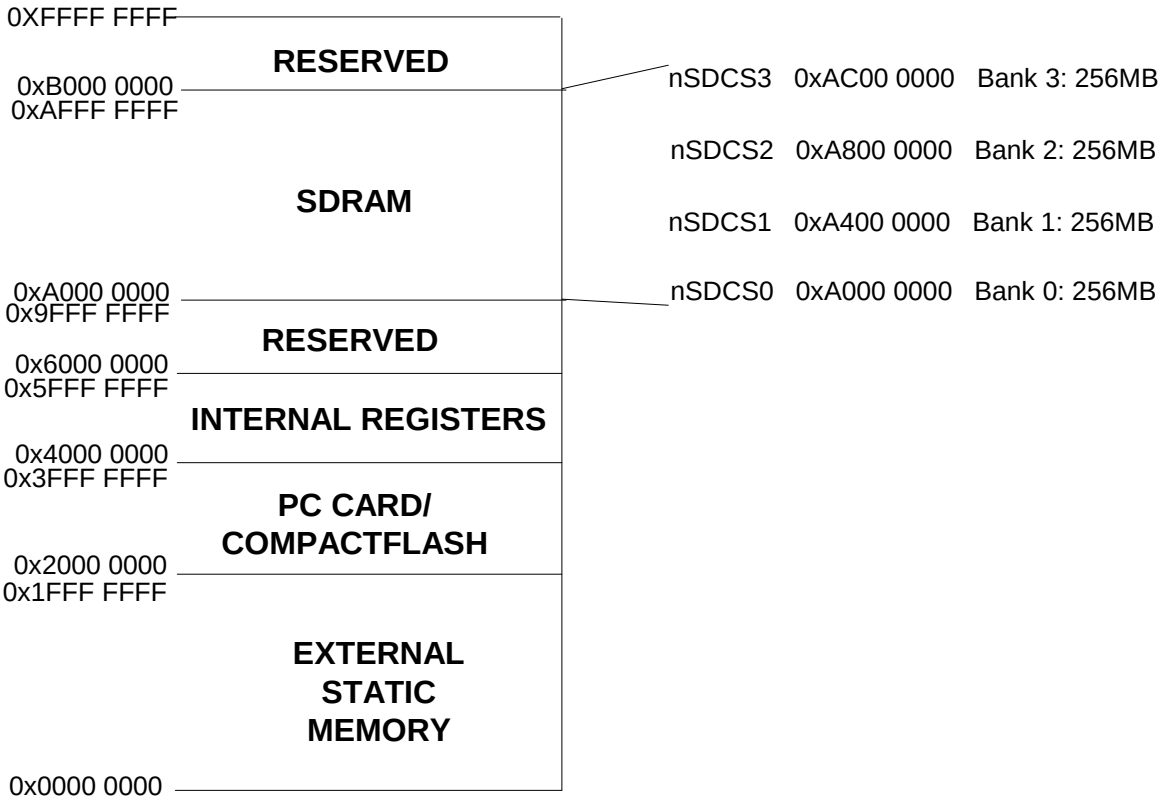


Figure 4.1: PXA270 SDRAM Memory Map

4.2 External Static Memory Map

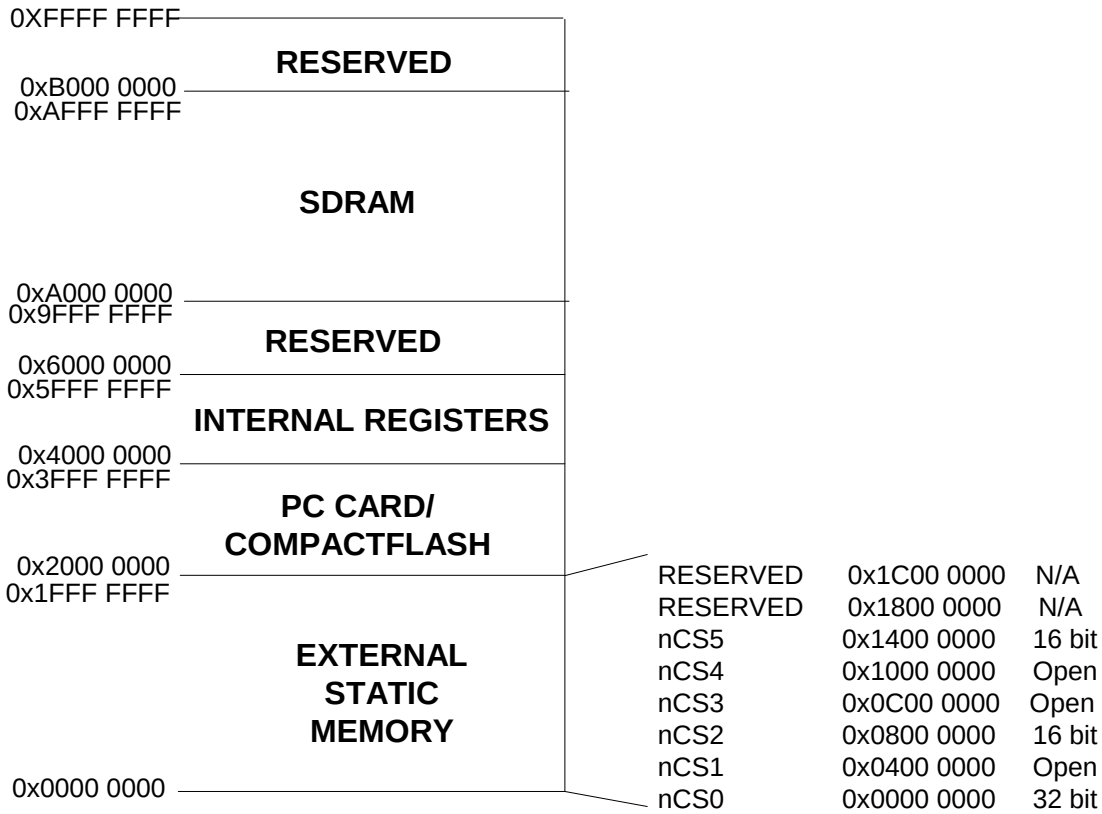


Figure 4.2: PXA270 Static Memory Map

NOTE: The bit numbers refer to the bank width at reset.

4.2.1 SOM Static Memory Map Description

The table below indicates what each bank of external static memory is being used for on the SOM.

Chip Select	Bank	Start Address	Memory Description
nCS5	5	0x1400 0000	IO Controller Peripherals (Slow[1])
nCS4	4	0x1000 0000	Open
nCS3	3	0x0C00 0000	Open
nCS2	2	0x0800 0000	IO Controller Peripherals (Fast[1]) / Boot Device (Flash or Off-Board)
nCS1	1	0x0400 0000	Open
nCS0	0	0x0000 0000	Boot Device (Flash or Off-Board)

Notes: CPLD peripherals are components that get a decoded chip select from the CPLD (e.g., CPLD memory-mapped registers, onboard SMSC 91C111 Ethernet controller). These peripherals are separated into two different chip select banks due to the difference in timing: slow and fast. Please see the *PXA270-10 IO Controller Specification* document for details.

4.2.2 Chip Select 5 (CS5) – CPLD Peripherals (slow timing)

The table below indicates how the CPLD decodes chip select 5. For more detailed information see the *PXA270-10 IO Controller Specification*.

Address Range	Memory Block Description	Size
0x1400 0000 – 0x14FF FFFF	CF Chip Select	16MB
0x1500 0000 – 0x15FF FFFF	ISA-like Bus Chip Select	16MB
0x1600 0000 – 0x16FF FFFF	Reserved	16MB
0x1700 0000 – 0x17FF FFFF	Open	16MB

4.2.3 Chip Select 2 (CS2) – CPLD Peripherals (fast timing)

The table below indicates how the CPLD decodes chip select 2. For more detailed information see the *PXA270-10 IO Controller Specification*.

Address Range	Memory Block Description	Area Size
0x0800 0000 – 0x0800 0003	Card Engine Control Reg	4Byte
0x0800 0004 – 0x0800 000F	Peripheral Reg0	12Byte
0x0800 0010 – 0x0800 0013	Peripheral Reg1	4Byte
0x0800 0014 – 0x0800 001F	IO Controller Code Revision Reg	12Byte
0x0800 0020 – 0x0800 0023	EEPROM SPI Reg	4Byte
0x0800 0024 – 0x0800 002F	Mode Reg	12Byte
0x0800 0030 – 0x0800 0033	GPIO Reg	4Byte
0x0800 0034 – 0x0800 003F	Reserved	12Byte
0x0800 0040 – 0x0800 0043	Interrupt Mask Reg	4Byte
0x0800 0044 – 0x0800 004F	Reserved	12Byte
0x0800 0050 – 0x0800 0053	Interrupt Reg	4Byte
0x0800 0054 – 0x0800 005F	Reserved	12Byte
0x0800 0060 – 0x0800 0063	BSP1 Support Reg	4Byte
0x0800 0064 – 0x0800 006F	BSP2 Support Reg	12Byte
0x0800 0070 – 0x0800 0073	Reserved	4Byte
0x0800 0074 – 0x08FF FFFF	Reserved	16MByte – 102Byte
0x0900 0000 – 0x09FF FFFF	Wired LAN Chip Select	16MByte
0x0A00 0000 – 0x0AFF FFFF	External Fast_nCS	16MByte
0x0B00 0000 – 0x0BFF FFFF	Flash_nCS when uP_MODE3 = 0 Boot_nCS when uP_MODE3 = 1	16MByte

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs – all GPIOs on the PXA270 can be configured as either inputs or outputs – or active low/high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups / pull downs).

In addition, keep in mind that the following mode line numbers on the SOM do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SODIMM 144-Pin Descriptions

J1C Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 Mb/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I/O	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of volatile memory. Refer to the reset description found in Section 3.2.1 for more information on how this signal is driven. Every peripheral on the SOM with a reset line is reset with the assertion of this signal because the PXA270 asserts uP_nRESET_OUT (nRESET_OUT) when MSTR_nRST (nRESET) is driven low. Refer to PXA270 processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V_uP_BATT through a 10K resistor.
3	ETHER_RX(+)	I	This input pair receives 10/100 Mb/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4	uP_nWAKEUP/nRESET	I	Active Low. SW can use this signal to initiate a soft reset (manual reset) when the CPU is in Run state. It can also function as an nWAKEUP to take the processor out of a low power state. This signal is pulled up to 3.3V_uP_BATT through a 33K resistor.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nCS	O	Active Low. Chip select for area 2 of PXA270-10 memory, the "fast" peripheral chip select area. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and decodes an address that relates to the FAST_nCS, it asserts FAST_nCS.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).
8	SLOW_nCS	O	Active Low. Chip select for area 5 of PXA270-10 memory, the “slow” peripheral chip select area. See memory map for details. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and decodes an address that relates to the SLOW_nCS, it asserts SLOW_nCS.
9	DGND	I	Digital Ground (0V)
10	VIDEO_nCS (uP_nCS1)	O	Active Low. Chip select for area 1 of PXA270-10 memory. This is the "video" chip select area. This signal is not used by Logic BSPs and is available for users. See memory map for details.

J1C Pin #	Signal Name	I/O	Description
11	nACT_LED/LAN_LED1	O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
12	BOOT_nMCS	O	Active Low. This signal is the chip select for boot ROM in area 0 when uP_MODE3 is low. When uP_MODE3 is high, this signal is the chip select for a specific memory mapped address in the fast chip select area of PXA270-10 memory. See memory map for details.
13	nLNK_LED/LAN_LED2	O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR	O	Active Low. The ISA bus master or DMA controller drives the signal to communicate the presence of valid write data on the data bus. A peripheral may use this signal to latch the data in. See the PXA270-10 IO Controller Specification for further details.
15	nSTANDBY	I	Active Low. CPU power mode signal. Software can use nSTANDBY signal to make the SOM enter Standby state (hardware power down), PXA270 Deep Sleep Mode, where the contents of the SDRAM are placed in self-refresh and will be maintained. From standby, run is entered in response to a rising edge on nWAKEUP, or other internal or external wakeup events. Software must be implemented in order for this signal to operate properly. This signal is pulled up to 3.3V_uP_BATT through a 10K resistor.
16	nIORD (uP_nMRD)	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle. See the PXA270-10 IO Controller Specification for further details.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	3.3V_IN	I	Peripheral Power Supply (3.3V) controlled by SYS_EN. The 3.3V_IN power supply requires a minimum of 300 uF bulk capacitance.
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid or the processor data bus is in use. See the PXA270-10 CPLD IO Controller Specification for further details.
21	uP_nWAKEUP (uP_nWAKEUP/nRESET)	I	This CPU power mode signal causes Run state to be entered from Suspend or Standby state if implemented in software. This signal is pulled up to 3.3V_uP_BATT through a 10K resistor.
22	nCHRDY	I	Active Low. The I/O channel ready signal line serves to drive the asynchronous ready signal on the CompactFlash circuit low when additional cycle time is required. Push/Pull or open drain assertion of this signal are acceptable. This signal is pulled up to 3.3V through a 10K resistor.
23	uP_nIRQD	I	Software can use as a hardware interrupt on PXA270-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 33K resistor.
24		NC	No internal connection (not implemented on the PXA270-10)
25	uP_nIRQC	I	Software can use as a hardware interrupt on PXA270-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 33K resistor.
26		NC	No internal connection (not implemented on the PXA270-10)

J1C Pin #	Signal Name	I/O	Description
27	uP_nIRQB	I	Software can use as a hardware interrupt on PXA270-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 33K resistor.
28	uP_nTRST	I	Active Low. Driven low during power on in order to reset JTAG module. This signal is pulled up to 3.3V_uP_BATT through a 10K resistor.
29	uP_nIRQA	I	Software can use as a hardware interrupt on PXA270-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 33K resistor.
30	uP_TMS	I	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V_uP_BATT through a 33K resistor.
31		NC	No internal connection (not implemented on the PXA270-10)
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use.
33		NC	No internal connection (not implemented on the PXA270-10)
34	uP_TDI	I	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V_uP_BATT through a 33K resistor.
35		NC	No internal connection (not implemented on the PXA270-10)
36	uP_TCK	I	JTAG Test Clock Input. May leave unconnected if not using the JTAG port. This signal is pulled down to DGND through a 33K resistor.
37	uP_nWAIT	I	Active low. This is the processor's RDY signal. This signal is used by the VLIO memory area to extend bus cycles beyond standard wait state cycles. This signal is also driven low by the ISA and CF I/O Ready signal in the CPLD. For more information, see the PXA270 IO Controller Specification. This signal is pulled up to 3.3V through a 4.75K resistor.
38	uP_MODE3	I	Boot select signal (0 = external boot device, 1 = on-board flash). This is accomplished in the CPLD: if signal uP_MODE3 is high, then flash_nCS = uP_nCS0 and BOOT_nCS = uP_nCS2 and vice-versa if uP_MODE3 is low. This defaults to the on-board flash if left unconnected (pulled to 3.3V through a 33K resistor).
39	uP_UARTA_RTS	O	Ready to Send line for the UART2 interface.
40	uP_MODE2	I	LogicLoader software reads this pin to determine whether or not to run any stored scripts. Tying this signal low will prevent Logic Loader from running scripts at boot time. This pin can also be used as a General Purpose input and read from the CPLD register.
41	uP_UARTA_CTS	I	UART 2 clear to send on the PXA270-10.
42		NC	No internal connection (not implemented on the PXA270-10)
43	uP_UARTA_TX	O	UART 2 transmit output signal. This signal is pulled up to 3.3V through a 10k resistor.
44	uP_MODE0	I	<table><tr><td>Mode0</td><td>Bus Width</td></tr><tr><td>0</td><td>32-bit</td></tr><tr><td>1</td><td>16-bit</td></tr></table> Mode0 defaults to low if left unconnected (pulled to GND through a 33K resistor).
45	uP_UARTA_RX	I	UART 2 receive input signal on the PXA270.
46	uP_DREQ1	I	The DMA Request 1 line. This signal is pulled to 3.3V through a 33K resistor.
47	uP_UARTA_DTR	O	UART 2 data terminal ready signal on the PXA270.
48	uP_DREQ0	I	The DMA Request 0 line. This signal is pulled to 3.3V through a 33K resistor.
49	uP_UARTA_DSR	O	UART 2 data set ready on the PXA270.

J1C Pin #	Signal Name	I/O	Description
50	uP_nRESET_OUT	O	nRESET_OUT signal from PXA270. This signal is used to bring devices out of reset a delayed time after MSTR_nRST is asserted. All onboard devices are reset by this signal. User devices that require reset assertion and are connected to the card engine should use this signal. See reset section.
51	nSUSPEND	I	Active low. Software can use this signal to suspend PXA270 operations. This pin is pulled up to 3.3V by a 33k resistor. Software is required for proper suspend operation.
52		NC	No internal connection (not implemented on the PXA270-10)
53	uP_AUX_CLK	O	This signal is a GPIO by default. It can be setup as an AUX_CLK. See the PXA270 Developer's Manual for more information.
54	uP_DACK1	O	The DMA Acknowledge 1 line.
55	DGND	I	Digital Ground (0V)
56	uP_DACK0	O	The DMA Acknowledge 0 line.
57	VCORE_IN	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE varies based on processor and CPU operating mode.
58	VCORE_IN	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE varies based on processor and CPU operating mode.
59	VCORE_IN	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE varies based on processor and CPU operating mode.
60	VCORE_IN	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE varies based on processor and CPU operating mode.
61	3.3V_uP_BATT	I	Supplies power to the VCC_BATT signal on the PXA270 and powers the PXA270 power management unit. This signal should be maintained at all times to keep RTC contents. This supply must be powered to start the power manager on the processor. Recommend leaving this supply as the only powered supply during Standby power down mode for lowest power consumption
62	3.3V_uP_SDRAM	I	SDRAM Power Supply (3.3 V) (on during low power states). Recommend leaving this supply as the only powered supply during Standby power down mode if the SDRAM contents must be maintained.
63	3.3V_uP_SDRAM	I	SDRAM Power Supply (3.3 V) (on during low power states). Recommend leaving this supply as the only powered supply during Standby power down mode if the SDRAM contents must be maintained.
64	3.3V_uP_SDRAM	I	SDRAM Power Supply (3.3 V) (on during low power states). Recommend leaving this supply as the only powered supply during Standby power down mode if the SDRAM contents must be maintained.
65	uP_SPI_FRM	O	Software controlled SPI framing signal. This signal may be used by application software to frame SPI data transmission or reception.
66	uP_BUS_CLK	O	Synchronous Memory Clock. This clock operates at 52MHz and is connected to the flash as well as the CPLD.
67	uP_SPI_TX	O	This output transmits synchronous SPI data.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_RX	I	This input receives synchronous SPI data. This signal is pulled up to 3.3V through a 33K resistor.
70	uP_nRAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into row addressing mode.
71	uP_SPI_SCK	O	SPI clock signal.
72	uP_nCAS	O	Synchronous Memory Column Address Strobe Signal. This signal is used in synchronizing all SDRAM into column addressing mode.
73	uP_MD0	I/O	Buffered Data Bus bit 0.

J1C Pin #	Signal Name	I/O	Description
74	uP_nMWE3	O	This is the buffered Byte Lane Enable 3 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths. Active low only on writes.
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	uP_nMWE2	O	This is the buffered Byte Lane Enable 2 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths. Active low only on writes.
77	uP_MD2	I/O	Buffered Data Bus bit 2.
78	uP_nMWE1	O	This is the buffered Byte Lane Enable 1 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths. Active low only on writes.
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0	O	This is the buffered Byte Lane Enable 0 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths. Active low only on writes.
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	Active low. This buffered signal is the processor's write enable line.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD	O	Active low. This buffered signal is the read strobe that latches data output from external peripherals.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection (not implemented on the PXA270-10)
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88	uP_MA27 (MFP41 - GPIO36/FFDSR/ USB_P2_8/SSPSFRM2/KP_MKIN3/FFTXD)	I/O	GPIO36
89	DGND	I	Digital Ground (0V)
90	uP_MA0	O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	O	Buffered Address Bus bit 8.
107	3.3V_IN	I	Peripheral Power Supply (3.3V) controlled by SYS_EN. The 3.3V_IN power supply requires a minimum of 300 uF bulk capacitance.
108	uP_MA9	O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	O	Buffered Address Bus bit 10.
111	uP_MD16	I/O	Buffered Data Bus bit 16.
112	uP_MA11	O	Buffered Address Bus bit 11.
113	uP_MD17	I/O	Buffered Data Bus bit 17.
114	uP_MA12	O	Buffered Address Bus bit 12.
115	uP_MD18	I/O	Buffered Data Bus bit 18.

J1C Pin #	Signal Name	I/O	Description
116	uP_MA13	O	Buffered Address Bus bit 13.
117	uP_MD19	I/O	Buffered Data Bus bit 19.
118	uP_MA14	O	Buffered Address Bus bit 14.
119	uP_MD20	I/O	Buffered Data Bus bit 20.
120	uP_MA15	O	Buffered Address Bus bit 15.
121	uP_MD21	I/O	Buffered Data Bus bit 21.
122	uP_MA16	O	Buffered Address Bus bit 16.
123	uP_MD22	I/O	Buffered Data Bus bit 22.
124	uP_MA17	O	Buffered Address Bus bit 17.
125	uP_MD23	I/O	Buffered Data Bus bit 23.
126	uP_MA18	O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	uP_MA19	O	Buffered Address Bus bit 19.
129	uP_MD24	I/O	Buffered Data Bus bit 24.
130	uP_MA20	O	Buffered Address Bus bit 20.
131	uP_MD25	I/O	Buffered Data Bus bit 25.
132	uP_MA21	O	Buffered Address Bus bit 21.
133	uP_MD26	I/O	Buffered Data Bus bit 26.
134	uP_MA22	O	Buffered Address Bus bit 22.
135	uP_MD27	I/O	Buffered Data Bus bit 27.
136	uP_MA23	O	Buffered Address Bus bit 23.
137	uP_MD28	I/O	Buffered Data Bus bit 28.
138	uP_MA24	O	Buffered Address Bus bit 24.
139	uP_MD29	I/O	Buffered Data Bus bit 29.
140	uP_MA25	O	Buffered Address Bus bit 25.
141	uP_MD30	I/O	Buffered Data Bus bit 30.
142	nAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143	uP_MD31	I/O	Buffered Data Bus bit 31.
144	3.3V_IN	I	Peripheral Power Supply (3.3V) controlled by SYS_EN. The 3.3V_IN power supply requires a minimum of 300 uF bulk capacitance.

5.2 J1A Expansion Connector Pin Descriptions

J1A Pin #	Signal Name	I/O	Description
1	LCD_VSYNC	O	LCD VSYNC (TFT Signal).
2	LCD_HSYNC	O	LCD HSYNC (TFT Signal).
3	LCD_DCLK	O	LCD Panel Data Clock
4	GPIO87 - LDD17/ LCD_DON	O	LCD DON signal.
5	LCD_MDISP	O	LCD enable signal (TFT signal).
6	LCD_VEEEN	O	Active high. This signal is the enable for the LCD panel Vee.
7	LCD_VDDEN	O	Active high. This signal is the LCD panel Vcc enable.
8		NC	No internal connection (not implemented on the PXA270-10)
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the PXA270-10)
11		NC	No internal connection (not implemented on the PXA270-10)
12	GPIO86 - LDD16/PSAVE	O	LCD power save.
13		NC	No internal connection (not implemented on the PXA270-10)
14		NC	No internal connection (not implemented on the PXA270-10)

J1A Pin #	Signal Name	I/O	Description
15		NC	No internal connection (not implemented on the PXA270-10)
16		NC	No internal connection (not implemented on the PXA270-10)
17	STATUS_1	I/O	This signal is attached to GPIO on the CPLD. Software can use this signal to output status information on the SDK LEDs. See the *PXA270-10 IO Controller Specification* for more information.
18	STATUS_2	I/O	This signal is attached to GPIO on the CPLD. Software can use this signal to output status information on the SDK LEDs. See the *PXA270-10 IO Controller Specification* for more information.
19	uP_I2S/AC97_BITCLK	O	Clock signal to an AC97 compliant audio CODEC.
20	uP_I2S_CODEC_CLK/ AC97_nRESET	O	AC97 reset line to an AC97 compliant audio CODEC. This signal is pulled up to 3.3V through a 100K resistor.
21	uP_I2S/AC97_SYNC	O	This signal is the AC97 sync output to an AC97 compliant audio CODEC. This signal is pulled down to DGND through a 100K resistor.
22	uP_I2S/AC97_SD_IN	I	This signal is the AC97 input to the processor from the AC97 compliant audio CODEC.
23	uP_I2S/AC97_SD_OUT	O	This signal is the AC97 output from the processor to the AC97 compliant audio CODEC. This signal is pulled down to DGND through a 100K resistor.
24	DGND	I	Digital Ground (0V)
25	A/D1	I	This signal is the input to channel 1 of the CODECs 10-bit A/D converter.
26	A/D2	I	This signal is the input to channel 2 of the CODECs 10-bit A/D converter.
27	AGND	I	Analog Ground (0V)
28	MFP39 - A/D3	I	This signal is the input to channel 3 of the CODECs 10-bit A/D converter.
29	MFP40 - VREFDRV	O	This signal is the reference voltage for the headphone drivers.
30	3.3VA_IN	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line input of the audio CODEC.
32	CODEC_INR	I	Right channel stereo line input of the audio CODEC.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Please see the Philips Semiconductors UCB1400 Technical Datasheet for more details.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Please see the Philips Semiconductors UCB1400 Technical Datasheet for more details.
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	This is the Y+ position input to the four-wire resistive touch screen controller.
37	TOUCH_RIGHT	I	This is the Y- position input to the four-wire resistive touch screen controller.
38	TOUCH_BOTTOM	I	This is the X+ position input to the four-wire resistive touch screen controller.
39	TOUCH_TOP	I	This is the X-position input to the four-wire resistive touch screen controller.
40	3.3VA_IN	I	Analog Power Supply (3.3V)
41	R0 (R5)	O	The LCD data bus used to transmit data to the LCD module. RED 0 is connected to LDD15.
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1 is connected to LDD11.
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2 is connected to LDD12.
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3 is connected to LDD13.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4 is connected to LDD14.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5 is connected to LDD15.

J1A Pin #	Signal Name	I/O	Description
48	G0	O	The LCD data bus used to transmit data to the LCD module. GREEN 0 is connected to LDD5.
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1 is connected to LDD6.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2 is connected to LDD7.
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3 is connected to LDD8.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4 is connected to LDD9.
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5 is connected to LDD10.
54	B0 (B5)	O	The LCD data bus used to transmit data to the LCD module. BLUE 0 is connected to LDD4.
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1 is connected to LDD0.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2 is connected to LDD1.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3 is connected to LDD2.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4 is connected to LDD3.
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5 is connected to LDD4.
61	CF_nCE	O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word read/write to the card. See the *PXA270-10 IO Controller Specification* for further details. This signal is pulled up to 3.3V through a 33K resistor.
62	uP_PCC_RDYA	I	This signal is the PC Card ready signal input for a 2nd PCMCIA slot when 2 devices are used. This signal is pulled up to 3.3V through a 33K resistor.
63	CPLD_GPIO_1	I/O	This signal is a general purpose I/O. It is controlled by a memory-mapped address in the CPLD. See the *PXA270-10 IO Controller Specification* for further details.
64	CPLD_GPIO_2	I/O	This signal is a general purpose I/O. It is controlled by a memory-mapped address in the CPLD. See the *PXA270-10 IO Controller Specification* for further details.
65	uP_USB2_OVR_CRNT	I	Active low. This signal indicates an over current condition on the USB host. See SDK application board schematics for recommended external USB circuitry.
66	DGND	I	Digital Ground (0V)
67	uP_USB1_VBUS	I	Active high. This is the data carrier detect signal for the main USB port. It is used to determine whether or not the USB interface is currently in use. This signal is pulled down to digital ground through a 150K resistor.
68	uP_USB2_PWR_EN	O	Active high. Enables USB port 2.
69	uP_USB1_PWR_EN	O	Active low. Enables power supply for USB port 1.
70	uP_USB2_M	I/O	USB port 2 data I/O minus. Route as a differential pair with uP_USB2_P.
71	uP_USB2_P	I/O	USB port 2 data I/O plus. Route as a differential pair with uP_USB2_M.
72	uP_USB1_M	I/O	USB port 1 data I/O minus. Route as a differential pair with uP_USB1_P.
73	uP_USB1_P	I/O	USB port 1 data I/O plus. Route as a differential pair with uP_USB1_M.
74	BUFF_nOE	O	Active low. This signal is the output enable for the data and address buffers on the SOM. This signal is pulled up to 3.3V through a 10K resistor in order to ensure the buffers are tri-stated upon powering up the SOM. When low, the buffers are active. See the *PXA270-10 IO Controller Specification* for further details on how this signal is driven.
75	BUFF_DIR_ADDRESS	O	The BUFF_DIR_ADDRESS is low for the PXA270 SOM.

J1A Pin #	Signal Name	I/O	Description
76	BUFF_DIR_DATA	O	Controls the direction of the data lines through the two data bus buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle). See the *PXA270-10 IO Controller Specification* for further details.
77	DGND	I	Digital Ground (0V)
78	MIC_IN	I	This signal is the microphone input to the AC97 compliant audio CODEC. Please see the Philips Semiconductors UCB1400 Technical Datasheet for more details.
79	POWER_SENSE1	O	These two pins are used to set the core voltage of the SOM. Please reference the ZOOM SDK reference schematics for details on implementation if the design may require support for different SOMs.
80	POWER_SENSE2	O	These two pins are used to set the core voltage of the SOM. Please reference the ZOOM SDK reference schematics for details on implementation if the design may require support for different SOMs.

5.3 J1B Expansion Connector Pin Description

J1B Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	This is the test clock input for the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
2	CPLD_TDO	O	This signal transmits data out of the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
3	CPLD_TMS	I	This input indicates the mode of CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
4	CPLD_TDI	I	This input receives data on the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
5	uP_PCC_nOE	O	This signal is PC Card Output Enable, Attribute, and Common Memory space read control. This signal is pulled up to 3.3V through a 33K resistor.
6	uP_PCC_nWE	O	This signal is for PC Card Write Enable, Attribute and Common Memory space write control. This signal is pulled up to 3.3V through a 4.75K resistor. This signal is also used as the write enable for the VLIO memory interface.
7	uP_PCC_nIORD	O	This signal is for PC Card IO Read Output. This signal is pulled up to 3.3V through a 33K resistor.
8	uP_PCC_nIOWR	O	This signal is for PC Card IO Write Output. This signal is pulled up to 3.3V through a 33K resistor.
9	DGND	I	Digital Ground (0V)
10	uP_PCC_RESET	O	This signal is PC Card Reset Card 1. This signal is pulled up to 3.3V_uP_BATT through a 33K resistor.
11	PCC_nCE1B	O	This signal is PC Card Enable 1 and is used with PCC_nCE2B to decode low and high byte accesses for slot two only.
12	PCC_nCE2B	O	This signal is PC Card Enable 2 and is used with PCC_nCE1B to decode low and high byte accesses for slot two only.
13	PCC_nIOIS16	O	Active low. PCMCIA IOIS16 signal. When low, this specifies that either a 16-bit IO card or a write-protected memory-only card is being used.
14	uP_PCC_RDYB	I	This is the PC Card ready input for slot one in dual card mode. This signal is pulled up to 3.3V through a 33K resistor.
15	uP_PCC_nWAIT	I	This is the PC Card wait signal input in dual card mode. This signal is pulled up to 3.3V through a 33K resistor.

J1B Pin #	Signal Name	I/O	Description
16	uP_PCC_BVD2	I	This signal is the Battery Sense 2 signal and is connected to GPIO 105. This signal is pulled up to 3.3V through a 33K resistor.
17	uP_PCC_BVD1	I	This signal is the Battery Sense 1 signal and is connected to GPIO 98. This signal is pulled up to 3.3V through a 33K resistor.
18	uP_PCC_nCD2	I	This signal is connected to GPIO 106. It can be used to sense the Card Detect input 2. The processor should be interrupted when this signal goes low. This signal is pulled up to 3.3V through a 33K resistor.
19	uP_PCC_nCD1	I	This signal is connected to GPIO 107. It can be used to sense the Card Detect input 1. The processor should be interrupted when this signal goes low. This signal is pulled up to 3.3V through a 33K resistor.
20	uP_PCC_nREG	O	This signal is for PC Card Register Memory Accesses.
21	DGND	I	Digital Ground (0V)
22	uP_PCC_VS1	I	This is the PC Card Voltage Sense 1 signal. GPIO104
23	uP_PCC_VS2	I	This is the PC Card Voltage Sense 2 signal. GPIO103
24	PCC_nDRV	O	This is the PC Card drive output signal. This signal is pulled up to 3.3V through a 33K resistor. GPIO108
25	uP_PCC_PCDIR (BUFF_DIR_DATA)	O	This signal is used for PCMCIA buffer data direction control.
26	uP_DQM3	O	This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[24:31].
27	uP_DQM2	O	This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[16:23].
28	uP_DQM1	O	This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[8:15].
29	uP_DQM0	O	This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[0:7].
30	uP_IRTX/UARTC_TX	O	This is the IrDA Transmit signal, which is used for the Infrared Mode on UARTC.
31	uP_IRRX/UARTC_RX	I	This is the IrDA Receive signal, which is used for the Infrared Mode on UARTC. This signal is pulled up to 3.3V through a 33K resistor.
32	DGND	I	Digital Ground (0V)
33	MFP1 - GPIO93_KP_DKIN_0	I/O	This signal is the direct key 0 input from the direct keypad.
34	MFP2 - GPIO94_KP_DKIN_1	I/O	This signal is the direct key 1 input from the direct keypad.
35	MFP3 - GPIO95_KP_DKIN_2	I/O	This signal is the direct key 2 input from the direct keypad.
36	MFP4 - GPIO100_KP_MKIN_0	I/O	This signal is the matrix key row heading 0 input from the matrix keypad.
37	MFP5 - GPIO111/MMDAT3/MMCCS1	I/O	This is the MultiMediaCard Data 3 signal. This signal is pulled up to 3.3V through a 33K resistor.
38	MFP6 - GPIO110/MMDAT2/MMCCS2	I/O	This is the MultiMediaCard Data 2 signal. This signal is pulled up to 3.3V through a 33K resistor.
39	MFP7 - GPIO109/MMDAT1/MSSDIO	I/O	This is the MultiMediaCard Data 1 signal. This signal is pulled up to 3.3V through a 33K resistor.
40	MFP8 - GPIO101_KP_MKIN_1	I/O	This signal is the matrix key row heading 1 input from the matrix keypad.
41	uP_UARTB_TX	O	High Speed UART transmit output signal on the PXA270-10.
42	uP_UARTB_RX	I	High Speed UART receive input signal on the PXA270-10.
43	uP_UARTB_CTS	I	High Speed UART clear to send on the PXA270-10.
44	DGND	I	Digital Ground (0V)
45	uP_UARTB_RTS	O	High Speed UART request to send on the PXA270-10.
46	uP_IRTX/UARTC_TX	O	This is the IrDA Transmit signal, which is used for the Infrared Mode on UARTC.

J1B Pin #	Signal Name	I/O	Description
47	uP_IRRX/UARTC_RX	I	This is the IrDA Receive signal, which is used for the Infrared Mode on UARTC. This signal is pulled up to 3.3V through a 33K resistor.
48	MFP9 - GPIO112/MMC_CMD	I/O	This signal is the MultiMediaCard "Command" signal. This signal is pulled up to 3.3V through a 33K resistor.
49	MFP10 - GPIO102_KP_MKIN_2	I/O	This signal is the matrix key row heading 2 input from the matrix keypad.
50	MFP11 - GPIO92/MMC_DATA	I/O	This is the MultiMediaCard Data signal. This signal is pulled up to 3.3V through a 33K resistor.
51	MFP12 - GPIO32/MMC_CLK	I/O	This signal is the MultiMediaCard clock.
52	MFP13 - uP_USIM_CLK	O	This signal is the USIM clock.
53	MFP14 - uP_USIM_IO	I/O	This signal is the USIM IO data.
54	MFP15 - uP_USIM_VSO	O	This signal selects zero voltage on the USIM card power-supply pad.
55	DGND	I	Digital Ground (0V)
56	MFP16 - uP_USIM_DETECT	O	This signal is the USIM detect. This signal is pulled down to DGND through a 33K resistor.
57	MFP17 - uP_USIM_EN	O	This signal is the USIM enable.
58	MFP18 - uP_USIM_nRESET	O	Active low. This signal is the USIM reset.
59	MFP19 - GPIO117/SCL	I/O	This signal is the I2C Serial Clock Line.
60	MFP20 - PCC_nCE1A	O	Active low. This signal is the PCMCIA chip enable1 for slot A.
61	MFP21 - PWM0	I/O	DC-DC Converter 0 Output (Pulse Width Modulated)
62	MFP22 - PCC_nCE2A	O	Active low. This signal is the PCMCIA chip enable2 for slot A.
63	MFP23 - GPIO3/PWR_SCL	I/O	This signal is the Power I2C Serial Clock Line. This signal is pulled up to 3.3V_uP_BATT through a 33K resistor.
64	MFP24 - GPIO4/PWR_SDA	I/O	This signal is the Power I2C Data/Address. This signal is pulled up to 3.3V_uP_BATT through a 33K resistor.
65	MFP25 - GPIO13/CLK_EXT/ SSPTXD2/KP_DKIN7/KP_MKIN7	I/O	This signal is GPIO13.
66	DGND	I	Digital Ground (0V)
67	MFP26 - GPIO11/EXT_SYNC0/CHOUT0/ SSPRXD2/PWM_OUT2/USB_P3_1/48_MHZ	I/O	This signal is GPIO11.
68	MFP27 - PWM1	I/O	DC-DC Converter 1 Output (Pulse Width Modulated)
69	MFP28 - GPIO80/DREQ1/MBREQ/nCS4/PWM_OUT3	I/O	Active low. This is the Chip Select 4 signal for off-board use or any GPIO80 functions.
70	MFP29 - uP_SDCKE	O	This signal is the processors SDKE signal, which is used for accessing SDRAM.
71	MFP30 - GPIO118/SDA	I/O	This signal is the I2C Data/Address.
72	MFP31 - uP_nSDCS1	O	Active low. This signal is the processor's Synchronous Memory Chip Select 1.
73	MFP32 - VCC_USIM	I/O	This signal is the USIM VCC. It can be used to supply VCC to USIM if VCC is not supplied by the card engine.
74	MFP33 - PWR_EN	O	This signal enables the onboard low-voltage power areas. See power section for more details.
75	MFP34 - SYS_EN	O	This signal enables the onboard high-voltage power areas. See power section for more details.
76	MFP35 - GPIO84/SSPSCLK3	I/O	This is the Synchronous Serial Port 3 Clock signal.
77	DGND	I	Digital Ground (0V)
78	MFP36 - GPIO82/SSPSRXD3	I/O	This is the Synchronous Serial Port 3 Receive Data signal. This signal is pulled up to 3.3V through a 33K resistor.
79	MFP37 - GPIO81/SSPSTXD3	I/O	This is the Synchronous Serial Port 3 Transmit Data signal.
80	MFP38 - GPIO83/SSPSFRM3	I/O	This is the Synchronous Serial Port 3 Frame signal.

5.4 Multiplexed Signal Trade-Offs

5.4.1 J1C Connector SODIMM 144-Pin Multiplexing

J1C Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
4, 21	uP_nWAKEUP/nRESET	uP_nWAKEUP	Initiates wakeup	GPIO1	GPIO_nRESET
10	uP_nCS1	uP_nCS1 (VIDEO_nCS)	Chip Select 1 (Video Chip Select)	GPIO15	GPIO15
23	uP_IRQD	INT3	Interrupt 3 input	GPIO99	GPIO99
25	uP_IRQC	INT2	Interrupt 2 input	GPIO27	GPIO27
27	uP_IRQB	INT1	Interrupt 1 input	GPIO22	GPIO22
29	uP_IRQA	INT0	Interrupt 0 input	GPIO12	GPIO12
39	uP_UARTA_RTS	uP_UARTA_RTS	RTS signal for UART	GPIO41	GPIO41
41	uP_UARTA_CTS	uP_UARTA_CTS	CTS signal for UART	GPIO35	GPIO35
43	uP_UARTA_TX	uP_UARTA_TX	TX signal for UART	GPIO39	GPIO39
45	uP_UARTA_RX	uP_UARTA_RX	RX signal for UART	GPIO34	GPIO34
46	uP_DREQ1	uP_DREQ1	DREQ1 signal	GPIO97	GPIO97
47	uP_UARTA_DTR	uP_UARTA_DTR	DTR signal for UART	GPIO40	GPIO40
48	uP_DREQ0	uP_DREQ0	DREQ0 signal	GPIO20	GPIO20
49	uP_UARTA_DSR	uP_UARTA_DSR	DSR signal for UART	GPIO37	GPIO37
53	uP_AUX_CLK	uP_AUX_CLK	Auxiliary clock signal	GPIO9	GPIO9
54	uP_DACK1	uP_DACK1	DACK1 signal	GPIO96	GPIO96
56	uP_DACK0	uP_DACK0	DACK0 signal	GPIO21	GPIO21
65	uP_SPI_FRM	uP_SPI_FRM	SPI framing signal	GPIO24	GPIO24
67	uP_SPI_TX	uP_SPI_TX	SPI TX signal	GPIO25	GPIO25
69	uP_SPI_RX	uP_SPI_RX	SPI RX signal	GPIO26	GPIO26
71	uP_SPI_SCK	uP_SPI_SCK	SPI clock signal	GPIO23	GPIO23
88	MFP41 - GPIO36/ FFDSR/USB_P2_8/ SSPSFRM2/KP_MKIN3 /FFTXD	NA	NA	GPIO36	GPIO36

5.4.2 J1A Expansion Connector Pin Multiplexing

J1A Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
1	LCD_VSYNC	LCD_VSYNC	LCD Vertical Sync Pulse Output (TFT)	GPIO74	GPIO74
2	LCD_HSYNC	LCD_HSYNC	LCD Horizontal Sync Pulse Output (TFT)	GPIO75	GPIO75
3	LCD_DCLK	LCD_DCLK	LCD Clock	GPIO76	GPIO76
4	GPIO87 - LDD17/ LCD_DON	LCD_DON	LCD DON signal	GPIO87	GPIO87
5	LCD_MDISP	LCD_MDISP	TFT data enable	GPIO77	GPIO77
6	LCD_VEEEN	LCD_VEEEN	Digital supply enable	GPIO19	GPIO19
7	LCD_VDDEN	LCD_VDDEN	Digital supply enable	GPIO14	GPIO14
12	GPIO86 - LDD16/PSAVE	PSAVE	LCD power save	GPIO86	GPIO86
19	uP_I2S/AC97_BITCLK	AC97_BITCLK	AC97 Clock	GPIO28	GPIO28

J1A Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
20	uP_I2S_CODEC_CLK - AC97_nRESET	AC97_nRESET	AC97 reset signal	GPIO113	GPIO113
21	uP_I2S/AC97_SYNC	uP_I2S/AC97_SYNC	AC97 sync signal	GPIO31	GPIO31
22	uP_I2S/AC97_SD_IN	uP_I2S/AC97_SD_IN	AC97 in signal	GPIO29	GPIO29
23	uP_I2S/AC97_SD_OUT	uP_I2S/AC97_SD_OUT	AC97 out signal	GPIO30	GPIO30
41,47	R5	LDD15	LCD Data 15	GPIO73	GPIO73
42	R1	LDD11	LCD Data 11	GPIO69	GPIO69
43	R2	LDD12	LCD Data 12	GPIO70	GPIO70
45	R3	LDD13	LCD Data 13	GPIO71	GPIO71
46	R4	LDD14	LCD Data 14	GPIO72	GPIO72
48	G0	LDD5	LCD Intensity	GPIO63	GPIO63
49	G1	LDD6	LCD Data 6	GPIO64	GPIO64
50	G2	LDD7	LCD Data 7	GPIO65	GPIO65
51	G3	LDD8	LCD Data 8	GPIO66	GPIO66
52	G4	LDD9	LCD Data 9	GPIO67	GPIO67
53	G5	LDD10	LCD Data 10	GPIO68	GPIO68
54,60	B5	LDD4	LCD Data 4	GPIO62	GPIO62
56	B1	LDD0	LCD Data 0	GPIO58	GPIO58
57	B2	LDD1	LCD Data 1	GPIO59	GPIO59
58	B3	LDD2	LCD Data 2	GPIO60	GPIO60
59	B4	LDD3	LCD Data 3	GPIO61	GPIO61
62	uP_PCC_RDYA	uP_PCC_RDYA	PCMCIA ready slot 2	GPIO53	GPIO53
65	uP_USB2_OVR_CRNT	uP_USB2_OVR_CRNT	USB Port 2 Data Carrier Detect	GPIO88	GPIO88

5.4.3 J1B Expansion Connector Pin Multiplexing

J1B Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
5	uP_PCC_nOE	uP_PCC_nOE	PC Card Output Enable	GPIO48	GPIO48
6	uP_PCC_nWE	uP_PCC_nWE	PC Card Write Enable	GPIO49	GPIO49
7	uP_PCC_nIORD	uP_PCC_nIORD	PC Card IO Write Output	GPIO50	GPIO50
8	uP_PCC_nIOWR	uP_PCC_nIOWR	PC Card IO READ Output	GPIO51	GPIO51
10	uP_PCC_RESET	uP_PCC_RESET	PC Card Reset 1	GPIO10	GPIO10
13	PCC_nIOIS16	PCC_nIOIS16	PCMCIA IOIS16 Signal	GPIO57	GPIO57
14	uP_PCC_RDYB	uP_PCC_RDYB	PC Card slot 1 ready signal	GPIO52	GPIO52
15	uP_PCC_nWAIT	uP_PCC_nWAIT	PC Card wait signal	GPIO56	GPIO56
16	UP_PCC_BVD2	UP_PCC_BVD2	Battery Voltage Detect 2	GPIO105	GPIO105
17	UP_PCC_BVD1	UP_PCC_BVD1	Battery Voltage Detect 3	GPIO98	GPIO98
18	uP_PCC_nCD2	uP_PCC_nCD2	PC Card Detect 2 Input	GPIO106	GPIO106

J1B Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
19	uP_PCC_nCD1	uP_PCC_nCD1	PC Card Detect 1 Input	GPIO107	GPIO107
20	uP_PCC_REG	uP_PCC_REG	PC Card Register Memory Access	GPIO55	GPIO55
22	uP_PCC_VS1	uP_PCC_VS1	PC Card Voltage Sense 1 Input	GPIO104	GPIO104
23	uP_PCC_VS2	uP_PCC_VS2	PC Card Voltage Sense 2 Input	GPIO103	GPIO103
24	PCC_nDRV	PCC_nDRV	PC Card Drive Output	GPIO108	GPIO108
30	uP_IRTX/UARTC_TX	uP_IRTX/UARTC_TX	IrDA transmit signal	GPIO47	GPIO47
31	uP_IRRX/UARTC_RX	uP_IRRX/UARTC_RX	IrDA receive signal	GPIO46	GPIO46
33	MFP1 - GPIO93_KP_DKIN_0	KP_DKIN_0	Direct Key 0 input	GPIO93	GPIO93
34	MFP2 - GPIO94_KP_DKIN_1	KP_DKIN_1	Direct Key 1 input	GPIO94	GPIO94
35	MFP3 - GPIO95_KP_DKIN_2	KP_DKIN_2	Direct Key 2 input	GPIO95	GPIO95
36	MFP4 - GPIO100_KP_MKIN_0	KP_MKIN_0	matrix key row heading 0 input	GPIO100	GPIO100
37	MFP5 - GPIO111/MMDAT3/MMCCS1	MMDAT3	MMC Data3	GPIO111	GPIO111
38	MFP6 - GPIO110/MMDAT2/MMCCS0	MMDAT2	MMC Data2	GPIO110	GPIO110
39	MFP7 - GPIO109/MMDAT1/MSSDIO	MMDAT1	MMC Data1	GPIO109	GPIO109
40	MFP8 - GPIO101_KP_MKIN_1	KP_MKIN_1	matrix key row heading 1 input	GPIO101	GPIO101
41	uP_UARTB_TX	uP_UARTB_TX	High Speed UART TX Output Only	GPIO43	GPIO43
42	uP_UARTB_RX	uP_UARTB_RX	High Speed UART RX Input Only	GPIO42	GPIO42
43	uP_UARTB_CTS	uP_UARTB_CTS	High Speed UART RX Clear To Send	GPIO44	GPIO44
45	uP_UARTB_RTS	uP_UARTB_RTS	High Speed UART Request To Send	GPIO45	GPIO45
46	uP_IRTX/UARTC_TX	uP_IRTX/UARTC_TX	IrDA transmit signal	GPIO47	GPIO47
47	uP_IRRX/UARTC_RX	uP_IRRX/UARTC_RX	IrDA receive signal	GPIO46	GPIO46
48	MFP9 - GPIO112/MMC_CMD	MMC_CMD	MMC Command	GPIO112	GPIO112
49	MFP10 - GPIO102_KP_MKIN_2	KP_MKIN_2	matrix key row heading 2 input	GPIO102	GPIO102
50	MFP11 - GPIO92/MMC_DATA	MMC_DATA	MMC Data	GPIO92	GPIO92
51	MFP12 - GPIO32/MMC_CLK	MMC_CLK	MMC Clock	GPIO32	GPIO32
52	MFP13 - uP_USIM_CLK	uP_USIM_CLK	USIM Clock	GPIO91	GPIO91
54	MFP15 - uP_USIM_VS0	uP_USIM_VS0	0V on USIM power pad	GPIO114	GPIO114
56	MFP16 - uP_USIM_DETECT	uP_USIM_DETECT	USIM Detection	GPIO116	GPIO116
57	MFP17 - uP_USIM_EN	uP_USIM_EN	USIM Enable	GPIO115	GPIO115
58	MFP18 - uP_USIM_nRESET	uP_USIM_nRESET	USIM Reset	GPIO90	GPIO90
59	MFP19 - GPIO117/SCL	SCL	I2C Serial Clock Line	GPIO117	GPIO117
61	MFP21 - PWM0	PWM0	PWM0 signal	GPIO16	GPIO16
63	MFP23 - GPIO3/PWR_SCL	PWR_SCL	Power Serial Clock Line	GPIO3	GPIO3
64	MFP24 - GPIO4/PWR_SDA	PWR_SDA	Power Serial Data/Address	GPIO4	GPIO4

J1B Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
65	MFP25 - GPIO13/CLK_EXT/SSPTXD2/ KP_DKIN7/KP_MKIN7	GPIO13	GPIO13	GPIO13	GPIO13
67	MFP26 - GPIO11/EXT_SYNC0/ CHOUT0/SSPRXD2/ PWM_OUT2/USB_P3_1/48_M HZ	SSPRXD2	SSP RX Data 2	GPIO11	GPIO11
68	MFP27 - PWM1	PWM1	PWM1 signal	GPIO17	GPIO17
69	MFP28 - GPIO80/DREQ1/MBREQ/ nCS4/PWM_OUT3	nCS4	Chip Select 4	GPIO80	GPIO80
71	MFP30 - GPIO118/SDA	SDA	I2C Serial Data/Address	GPIO118	GPIO118
76	MFP35 - GPIO84/SSPSCLK3	SSPSCLK3	Baseband Clock	GPIO84	GPIO84
78	MFP36 - GPIO82/SSPSRXD3	SSPSRXD3	Baseband Receive	GPIO82	GPIO82
79	MFP37 - GPIO81/SSPSTXD3	SSPSTXD3	Baseband Transmit	GPIO81	GPIO81
80	MFP38 - GPIO83/SSPSFRM3	SSPSFRM3	Baseband Frame	GPIO83	GPIO83

6 Mechanical Specifications

6.1 Interface Connectors

The PXA270-10 SOM connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SODIMM connector must be 3.7mm mating height.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	SOM P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

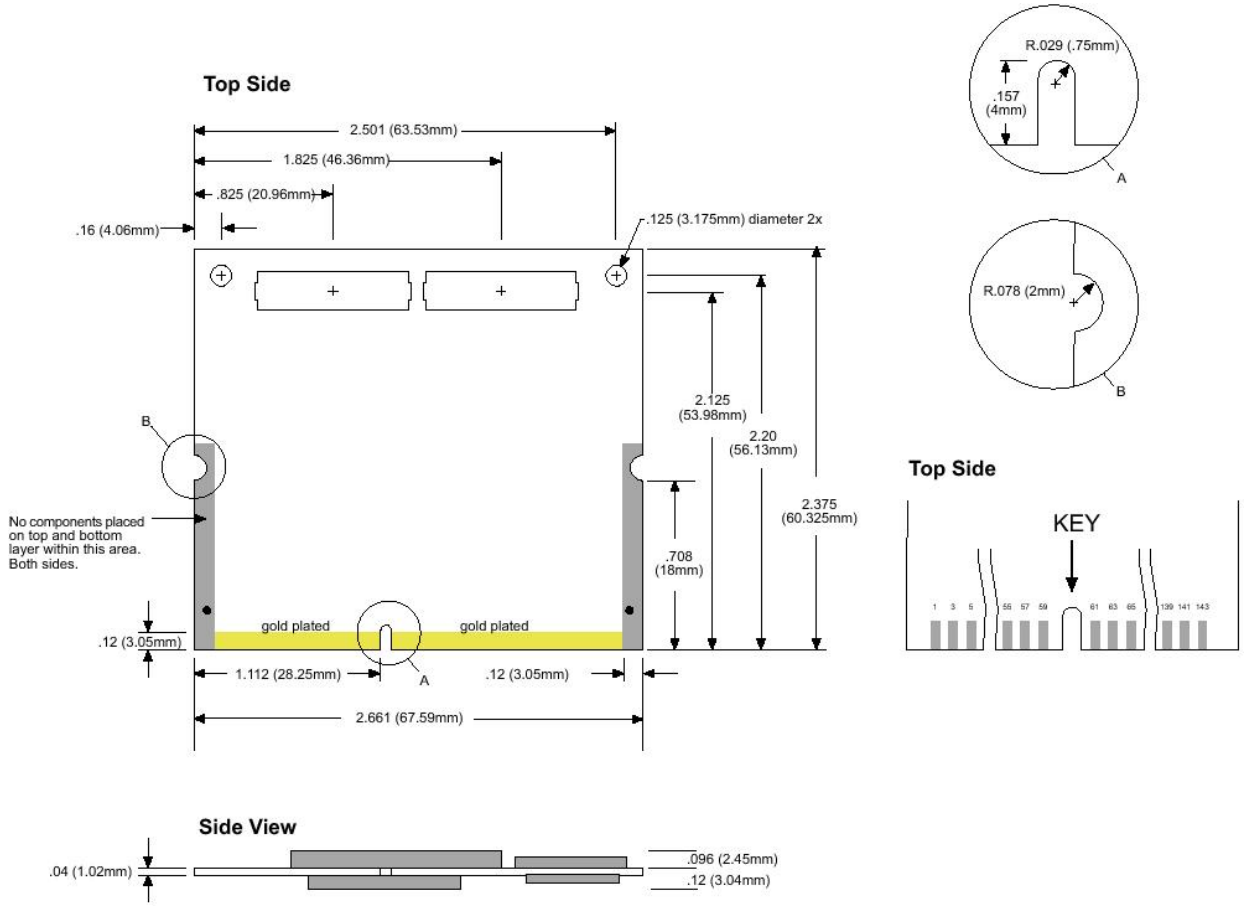


Figure 6.1: SOM Mechanical Drawing

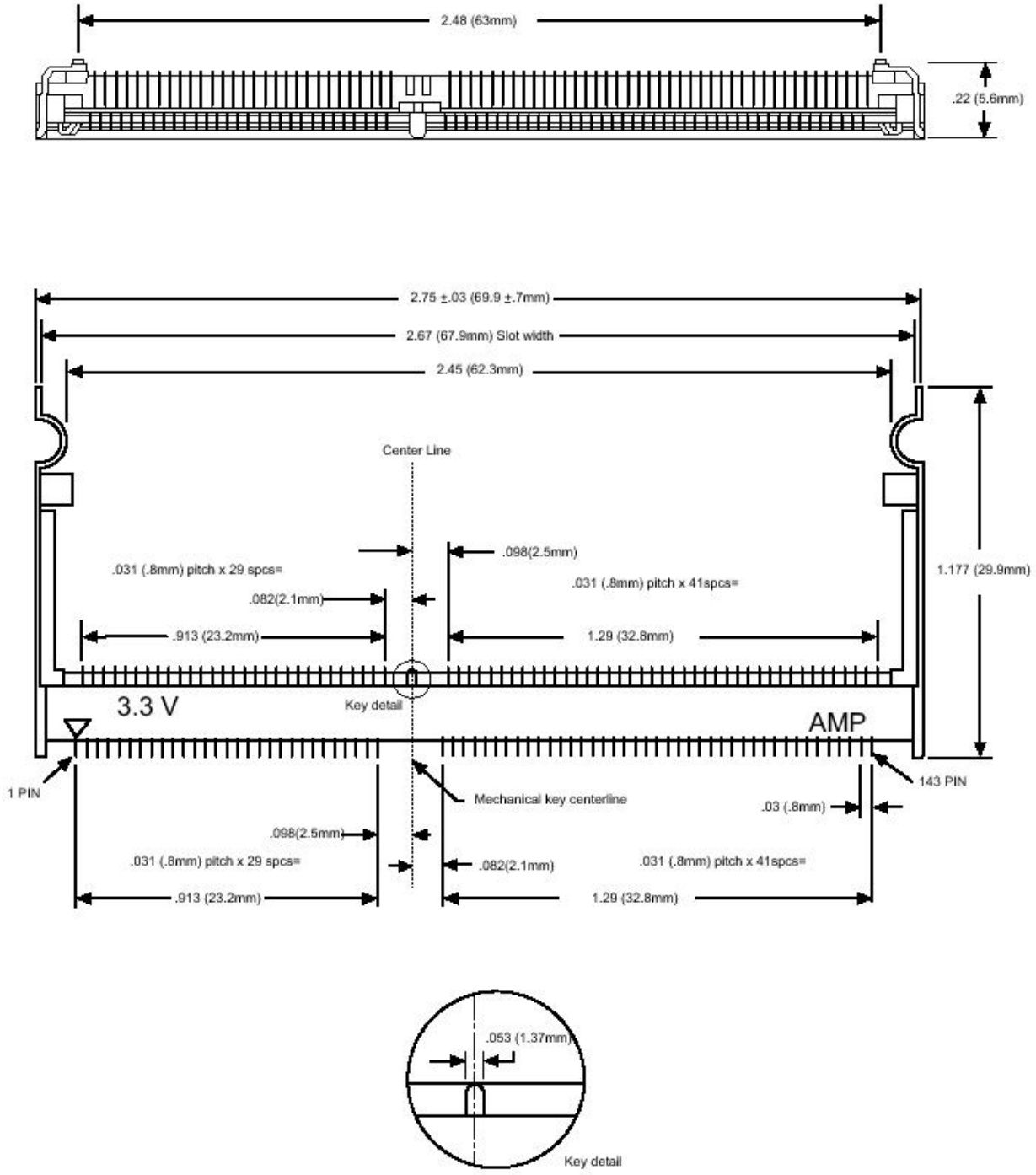


Figure 6.2: SODIMM Connector Specification

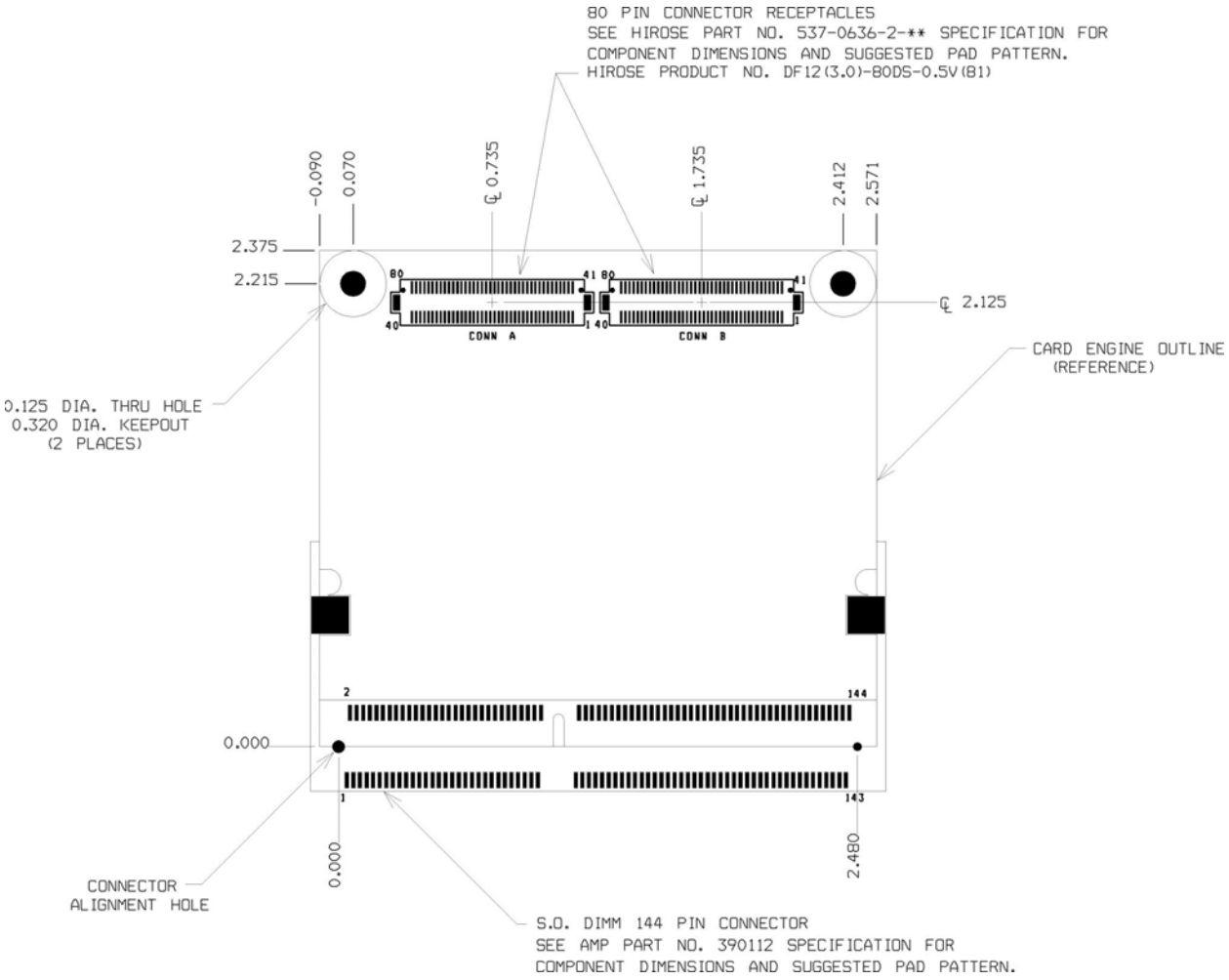


Figure 6.3: Recommended PCB Layout

